SiC Power Device Hammer and Burn-In System

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Abstract

The outstanding switching characteristics of SiC MOSFETs have enabled the power devices in many high-end applications. The industry adoption of SiC MOSFETs has accelerated significantly in the past couple years and outpaced the creation of SiC JEDEC standard (JC-70.2). Currently, manufacturers basically follow Si MOSFET JEDEC standards to qualify SiC MOSFETs with supplemental tests to ensure good device reliability. Among them, applicationoriented supplemental tests are important ones. This paper shares a production-grade application test system design. The system emulates real converter operations, including hard switching and soft switching, and stresses power devices at set conditions for device development and product screening purposes. The system uses a power cycling topology to minimize energy consumption.

1. Introduction

The emergence of SiC diodes in the early 20's is a milestone of power device evolution, which has changed application design practice and improved power conversion performance ever since. After almost two decades' development, the SiC technology is getting more mature and the second member of SiC power device family, SiC MOSFET, is now at the early stage of production. Compared with Si, SiC is much harder. It is the second hardest material known on the earth, just next to diamond. It is more difficult to process and its material quality, in terms of purity and defect rate, is yet as good as Si. Due to SiC's superior material characteristics, electrical field can be designed to 10 times higher than Si while growing gate oxide SiO2 on SiC is not as easy as and as perfect as the growing on Si, which makes SiC gate oxide design more critical to SiC MOSFET quality. Asymmetrical gate voltage, Vth drafting, bipolar degradation, etc, are new or more serious issues to SiC MOSFET design. It requires new gualification

procedure and standards to ensure products reliable. On application end, the early-stage's SiC have demonstrated MOSFETs outstanding performance. Tesla Model 3 electrical vehicle's successful use of SiC MOSFETs has accelerated industry adoption significantly. EV charger stations, EV on-board chargers, micro-grids, PV, solid-state transformers and many new energy designs also have started using SiC MOSFETs in volume production. The fast grow of SiC applications in the past few years is probably beyond initial expectation and has outpaced its corresponding JEDEC creation. SiC MOSFET JEDEC Standard JC 70.2 is still at early draft stage and is yet able to provide device manufacturers a united and sustain qualification criteria. Despite of the difference between Si and SiC, the commonality of Si MOSFETs and SiC MOSFETs may still be a dominated factor, due to their physics and device structure similarity. MOSFET Currently, most SiC device manufacturers apply Si's JEDEC to SiC MOSFET qualification directly, but at the meantime, they also believe that additional tests are necessary, at least at the early stage of production, to ensure device's quality and reliability. Table-1 shows commercial Si MOSFET qualification tests and additional tests or test conditions for SiC MOSFETs.

Test	Si Conditions	SiC Conditions
HTRB	JEDEC	JEDEC
HV-	JEDEC	JEDEC
H3TRB	100V	80% Vds rating
HTGB	JEDEC	JEDEC
IOL	Not required	AEC-Q101
тс	JEDEC	JEDEC
	-55°C-150°C	-55°C-150°C /175°C
HAST	JEDEC	JEDEC

These tests are basically independent static tests. There is some disconnection between the tests and real applications. The real applications stress power MOSFETs with Vds bias, gate voltage, reverse dv_ds/dt, di/dt and recovery simultaneously at temperature. elevated Application-oriented supplemental tests would be able to help manufacturers to find device weakness, reproduce failure modes, estimate device application lifetime and screen devices. Such tests add more confidence on device reliability to both manufacturers and end users. This paper will introduce a production-grade SiC power device hammer and burn-in system, and discuss some design in detail. The following sections will include,

Hammer and Burn-in System Overview,

Sub-System Power Circuit,

Dynamic Rds_on Sensing,

Test Setup and Data Examples, and Conclusions.

2. SiC MOSFET Hammer and Burn-in System

A production-grade hammer and burn-in system is different from a double pulse circuit. The system should be able to support high volume power device stress and screening tests at set conditions, and key operation data can be logged and saved automatically. The system should also be energy saving.

2.1. Hammer and Burn-in System Overview

Fig. 1 shows a photo of a hammer and burn-in system. The system consists of multiple burn-in cabinets. Each cabinet accommodates 10 sub-system test boards, and each sub-system is able to stress 4 TO-247-3 or TO-247-4 SiC MOSFETs simultaneously. All sub-systems are connected to an Ethernet and communicate with a central controller PC. The central controller can set each cabinet operation conditions, including bus voltage, current, switching frequency, device case temperature and hard switching/ soft switching cycling time. Sub-systems, shown in Fig. 2 and 3, report temperature and Vds or Rds_on of each MOSFET, operating current, and circuit status periodically.



Fig. 1. Hammer and burn-in system photo



Fig. 2. Hammer and burn-in system diagram



Fig. 3. Sub- system photo

All set values and reported values are displayed on the central controller screen. The test conditions and measured data are logged and saved to a server for test analysis. The subsystem is designed to allow hot swapping. The sub-system board with failed devices can be removed and plugged in after fixed without powering down a whole cabinet.

2.2. Sub-System Power Circuit

To operate MOSFETs at rated current and application voltage, the processed power could be very significant. For instance, an 80mOhm 1200V MOSFET could process 20kW power. Energy consumption would be a big issue if production needs to burn-in hundreds of devices daily without recovering any energy. To solve this problem, this Hammer and Burn-in system uses energy recycling full bridge topology, as shown in Fig.4(a) to minimize the power consumption to less than 1/100 of the processed power.

To ensure the power drown from the system's DC source is equal to the power returned to the DC source, both left half-bridge and right half-bridge should operate at near 50% duty cycle. By controlling the duty cycle, the inductor current can flow in either direction. When the inductor current flows from left to right, as shown in Fig.4(b), Q1 and Q4 operate at hard-switching mode, and Q2 and Q3 operate at soft-switching (freewheeling) mode. When the current flows in the opposite direction, the four switching devices swap softswitching mode and hard switching mode coordinately. There is a deadtime between each half bridge's two MOSFETs. During the deadtime, the inductor current freewheels through the body diodes of the freewheel MOSFETs, which operate at soft switching mode. If the two freewheel MOSFETs are fully turned off, the freewheel current can be used to stress their body diodes for bipolar degradation test purpose. The two freewheel MOSFETs can be replaced by two diodes as well for diode stress test.



Fig. 4. (a) Power Circuit, (b) Positive current operation, (c) negative current operation

2.3. Dynamic Rds_on Sensing

Rds_on is one of the main parameters indicating MOSFET's health status. Rds_on could have a step or rapid increase at the end of the MOSFET lifetime, due to wire bonds breaking or waring out. Large Vth drift or other defect could lead to an abnormal Rds_on as well. To measure a MOSFET's Rds-on while the MOSFET is switching at a high frequency and high common mode voltage, it requires the circuit be high speed and isolated. Fig.5 shows the sensing circuit used in this system.



Fig. 5. High-speed isolated Vds sensing circuit

D1 and D2 are high voltage blocking diodes. To minimize Vds measurement error, the diodes' forward voltage should be matched well at 1mA forward current. To achieve mV measurement accuracy, the sensing circuit may need to be calibrated, especially at 2V area, where most MOSFET Vds is when stressed at rated current.

2.4. MOSFET Temperature Sensing

Accurate MOSFET temperature measurement is important for the system to control and operate at set conditions. However, for volume production screen, it is not practical and is expensive to measure each device's junction temperature. Instead. case temperature can be sensed relatively easily. Noncontact infrared sensors are found to be a good choice. The following is a test. An infrared sensor MLX90614ESF-BCC was used to sense a TO-247 MOSFET's plastic case temperature at die location, and a thermal coupler measured the device's metal tab directly. While the device is being heated up by conducting a current, both temperatures were recorded, as shown in Fig. 5. With no air flow on a TO-247 device surface, the measured plastic case temperature matches fairly well with the metal case temperature. The error is with 4°C. If both measurements are accurate, the infrared data would be more close to the junction temperature due to temperature gradient caused by heat dissipating through its heatsink.



Fig. 6. Temperature measurement comparison

2.3. Test Setup and Data Examples

The system is fully GUI configurable. Each cabinet can be configured independently. Fig. 7 shows the system configuration window. Besides current values and operating time, current ramp-up and ramp-down time, over-temperature protection and over-current protection can be set as well.



Fig. 7. System configuration window



Fig. 8. System monitoring window

Fig. 8 shows the system's monitoring window. Each power device's temperature, Rds_on and current can

be monitored, logged and saved to a server automatically.

The following data, in Fig. 9, shows the burn-in test results of 12 early engineering samples of IVCT 1200V 80mOhm MOSFET. The devices were burned-in at 20A, 1000V and 125°C for 1000 hours. The devices' parameters were checked after 168 hour, 500 hour and 1000 hour's operation. The results indicate that the parameters shift slightly in the early operating hours and then become stable. A weak device was found gate-source shorted at 4-hour operating time point. The device was then sent out for diagnosis. FIB (Focused Ion Beam) slicing found the poly burn-out was caused by gate oxide process defect, as shown in the red circle in Fig. 10. Hammer and burn-in tests help developers locate problems quickly and correct design or process in time.



Fig.9. SiC MOSFET parameter stability test



Fig.10. SiC MOSFET defect root cause found

3. Conclusions

A SiC MOSFET hammer and burn-in system is introduced. The system is an effective tool to provide application-oriented supplemental tests for power device qualification. The system is also a valuable piece of equipment for developers to stress devices, find their weakness and improve design or process quickly. For production end, the system is able to screen devices before sending them to customers. The measure is an important step to ensure a good product quality, especially at the early stage of production.

References

[1] JEDCE JC-70, https://www.jedec.org/committees/jc-70.

[2] AEC-Q101, Rev. D1, "Failure Mechanism based Stress Test Qualification for Discrete Semiconductors in Automotive Applications," Sept. 2013.

[3] JEDEC Standard JESD94B, "Application Specific Qualification Using Knowledge Based Test Methodology," Oct. 2015.

[4] Tsunenobu Kimoto, James A.

Cooper, "Fundamentals of Silicon Carbide TechnologyGrowth, Characterization, Devices and Applications," Book, published by Wiley. [5] Donald A. Gajewski ; Brett Hull ; Daniel J. Lichtenwalner ; Sei-Hyung Ryu ; Eric Bonelli ; Habib Mustain,"SiC Power Device Reliability," APEC 2019.

[6] Sandeep R. Bahl, Daniel Ruiz and Dong Seup Lee, "Product-Level Reliability of GaN Devices", IEEE International Reliability Physics Symposium (IRPS), Apr. 2016.

[7] Sandeep R. Bahl, "Application-Relevant Qualification of Emerging Semiconductor Power Devices" APEC, March 2016.

[8] Ui-Min Choi ; Ionut Trintis ; Frede Blaabjerg ; Søren Jørgensen ; Morten Liengaard Svarre ,"Advanced Power Cycling Test for Power Module with On-line On-state VCE Measurement", 2015 IEEE Applied Power Electronics Conference and Exposition (APEC).

[9] Tsuyoshi Funaki," A Study on Performance Degradation of SiC MOSFET for Burn-in Test of Body Diode" 2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG).

[10] Joseph P. Kozak and Khai D. T. Ngo, "Trends in SiC MOSFET Threshold Voltage and ON-Resistance Measurements from Thermal Cycling and Electrical Switching Stresses," 10th International Conference on Integrated Power Electronics, March 2018.