SiC-Based High-Density Charger Plie Power Module Design

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Abstract

With more charger stations being built in urban commercial area, the physical size of charger piles becomes a main concern. Efficiency and power density of charger modules directly impact the charger stations investment capital and operation cost. This paper proposes a new AC/DC power conversion architecture, which uses a resonant DC transformer fed by a three-phase current-source PFC for battery charging. By eliminating DC bulk capacitors at the PFC output and employing SiC MOSFETs to simplify the power topologies and operate at higher switching frequency, both efficiency and density are improved. A 20kW charger module prototype was built to validate the concept and benchmark existing design.

1. Introduction

Electric vehicles (EVs) are a rapidly growing segment of the automotive industry owing to the improved technology, low carbon footprints, and government policy incentives. Currently, the electric vehicle industry is undergoing a technological transformation to improve vehicle range with charging infrastructure. Electric vehicle automakers and charge service enterprises are investing heavily in charging station infrastructure in order to support long-range battery electric vehicles and improve EV drivers' experience. Government incentives and automakers' initiatives for charging infrastructure development are the key factors driving the growth of the global electric vehicle charging stations market. The market is projected to reach around UDS 30 billion by 2027 at a CAGR of 36% from 2019 [1]. The level 3 DC charging station sub-segment is accounted for the largest share of the overall electric vehicle charging stations market and Asia pacific will command near 50% of the market during the forecast period. The large share of this segment is mainly attributed to rising demand for setting up of charging infrastructure at convenient urban commercial sites. Expensive commercial real estate drives investors and developers to squeeze charger pile sizes and increase charging power. That leads to the increasing demand of high density charger pile modules. To achieve high density design, the power converters need to operate at higher switching frequency with an equal or better efficiency.

Currently, charger pile modules of the state of art design and in volume production almost all use 650V Si MOSFETs in order to get a decent power density and efficiency out with an acceptable BOM cost. For a design with power over 6 kW, 3-phase input becomes necessary. Since the intermediate bus voltage exceeds 650V device derating requirement, three-level topologies or series-connected converters are the only choice for the design. Fig. 1 shows three main topologies used in 20kW-68kW commercial product designs. Fig. 1a is the topology using a Vienna PFC and a three-level phase-shifted full bridge DC/DC converter[2]; Fig.1b topology consists of a Vienna PFC and two series-connected three-phase LLC converters[3,4,5]; these two are isolated solutions. Fig. 1c shows a non-isolated solution with an I-type Vienna PFC and two series-connected multi-phase-interleaved buck converters. All of topologies basically use two-stage approach, which requires bulk capacitors to decouple the PFC and DC/DC stages. The bulk capacitors occupy around 20% of the module space, which becomes an obstacle to density improvement. Vienna PFC topologies have many advantages[6,7,8], but it seems there is no other good way to create an output voltage central point without using series-connected bulk capacitors. Complicity of the topologies is another issue, for which a large PCB space can be consumed by the gate driver circuitry. The non-isolated solution is a good approach to improve charger module density by eliminating high frequency power transformer. This solution would require an on-site AC power transformer to provide isolation and safety protection.

With SiC MOSFETs getting more mature and affordable, it opens up a new dimension for

engineers to use simple topologies and improve overall design. 1200V SiC MOSFETs found a sweet spot of applications where bus voltage is over 650V and operating frequency needs to be above 20kHz for hard switching and 50kHz for soft switching in general. High power density charger pile module would be a good playground for SiC MOSFETs to exercise their merits.

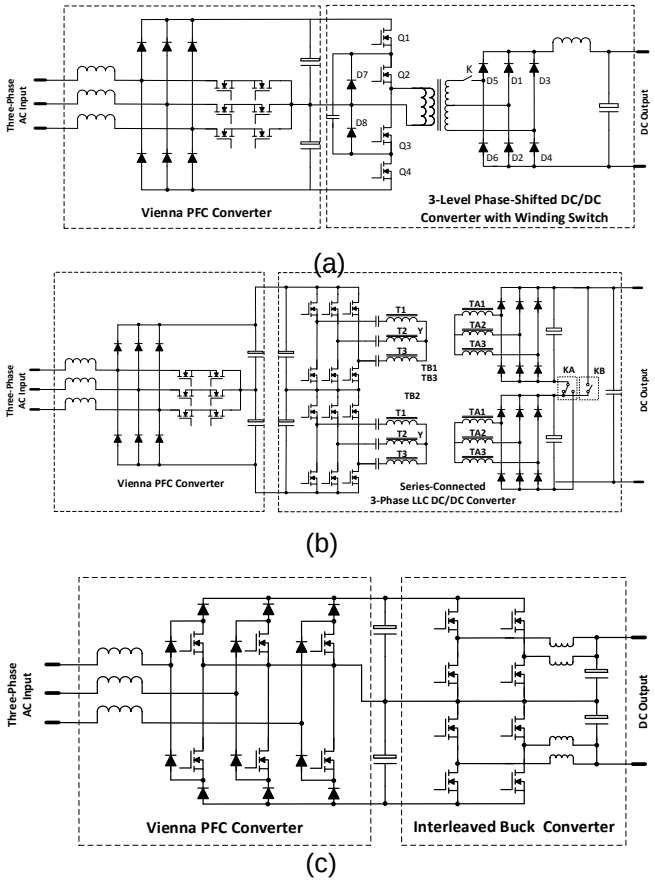


Fig.1. Main topologies used in commercial designs.

Now, to reduce or eliminate the bulk capacitors abovementioned, the question comes to what side effect it may have to charge a battery with AC line-frequency current ripple. [9,10,11] research found that current ripple under 5kHz had negligible impact on Li-ion battery performance and lifetime, and interestingly the test shows the batteries' impedance reaches the lowest value at around 100Hz. The authors took the advantage of this battery characteristic and proposed a fast pulse-charging method for Li-ion battery charging. There are not many literatures found on this topic, but it is reasonable to believe that hundreds' Hz current ripple at small percentage of charging current amplitude is safe for Li-ion battery charging.

Based on this assumption and by employing 1200V SiC MOSFETs, a new AC/DC power architecture is proposed for charge pile module design. The architecture uses an efficiency-optimized resonant DC transformer (DC-X) to isolate a three-phase current-source PFC's output current and to charge a battery pack directly. By using simpler but more efficient topologies and eliminating PFC output bulk capacitors, higher power density of charger module design becomes possible. For the detail discussion, this paper organizes coming sections as follows,

Section 2: High Density Power Architecture

Section 3: Power Stage and Control Design

Section 4: Experiment and Benchmarking

And the final part is Conclusions.

2. High Density Power Architecture

Since charger stations need to support a wide variety of electric vehicles charging, the charger output voltage is required to range from 330V to 750V generally. To shorten charging time, constant power control is preferred, which allows the chargers to provide a higher charging current when the battery SOC (State Of Charge) is low. However, constant power control adds a significant design challenge to engineers in terms of thermal design. With wide output voltage range requirement, traditional phase-shifted full bridge converters and LLC converters suffer from a higher power loss due to wider duty cycle or switching frequency regulation range. To mitigate this issue, [12] uses dual bridges with phase-shifted control to effectively achieve seamless series and parallel connection change of two rectifier outputs, but two phase current sharing is a remained challenge. [13,14,15] proposes wide-range input and/or constant-frequency LLC converters. These are good topologies, but adding two additional MOSFETs and corresponding control circuit each phase in this product design would cripple their advantages. The concept of DC-X battery chargers with a single-phase current source PFC has been evaluated by previous research and good results were achieved [16]. This paper extends the research to a three-phase input, wider battery voltage range and higher power level [17,18].

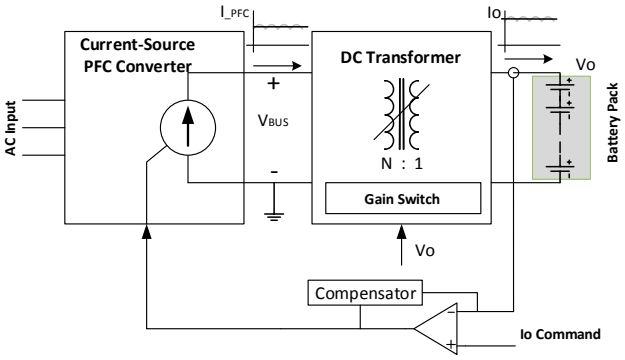


Fig.2. New AC/DC power architecture for battery charging.

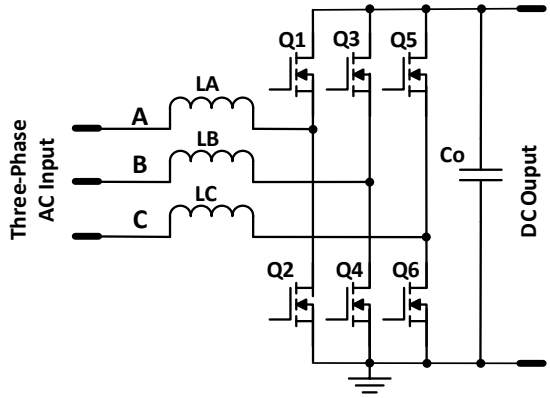


Fig.3. Traditional three-phase PFC circuit.

Fig. 2 shows the proposed power architecture, composed of a three-phase current source PFC and a gain-switchable DC transformer. The three-phase current-source PFC utilizes the traditional 3-phase PFC circuit, shown in Fig. 3, operating at current source mode. Each phase current maintains sinusoidal and in phase with its phase voltage. For the ideal case, the PFC output power can be expressed by,

$$Po = V_{rms} \cdot I_{rms} [\, Sin^2(\omega t) + Sin^2(\omega t + 2\pi/3) + Sin^2(\omega t - 2\pi/3)$$
$$= 3/2 \cdot V_{rms} \cdot I_{rms} \quad \ldots\ldots\ldots \quad (1)$$

It can be seen that there is no harmonic at the output. If the output is clamped to a DC voltage, the output current is a pure DC. Only a small high-frequency capacitor is required to absorb the output high frequency ripple. This is the advantage of the traditional three-phase PFC, which has long been overshadowed by other advanced topologies.

Since the second stage is a DC transformer stage, the PFC's output voltage is clamped by the reflected battery pack voltage. To accommodate 330V to 750V battery voltage range, the DC transformer needs to switch its gain somewhere at midpoint. Currently, EV battery voltages are basically divided into two groups at 500V boundary. A mechanical relay can be used to provide a reliable, low cost and low loss solution for the transformer winding switching and output voltage range selection, which has actually been used in current product designs.

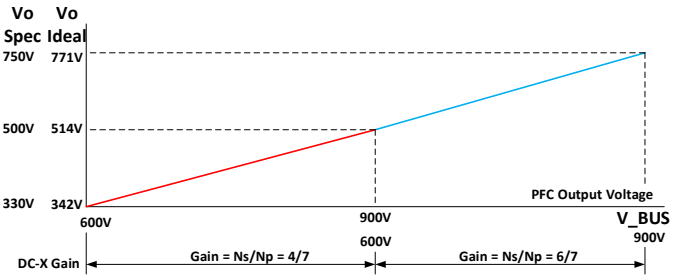


Fig.4. DC Transformer gain switching.

Fig.4 gives the relationship of battery voltage (Vo) and PFC output voltage (Vbus) with different DC-X gains. The DC-X gain is such selected that the PFC output range of 600V to 900V is just sufficient to cover the full EV battery voltage range. The maximum PFC output voltage selection is limited by 1200V SiC MOSFET voltage derating. Considering DC-X duty cycle loss and power train voltage drop, the ideal DC output voltage needs to be slightly higher than specified battery voltage at each corner case.

3. Power Stage and Control Design

A converter's power density is often limited by thermal hot spots. Magnetic components are the common places where hot spots occur, due to the difficulty to remove heat away from inner winding layers and winding-surrounded cores. Even thermal distribution is an effective measure to improve the power density. The three-Phase PFC uses three boost inductors, so it is relatively easy to manage its thermal. For the DC-X, interleaved structure is preferred. Besides thermal management, it makes a low profile design easier as well, for which further discussion will be provided in the next section.

Resonant converters have been widely used in DC transformer design. The converters operate at resonant frequency and achieve an optimal efficiency. Fig. 5 shows the selected topology for this 20kW DC-X design.

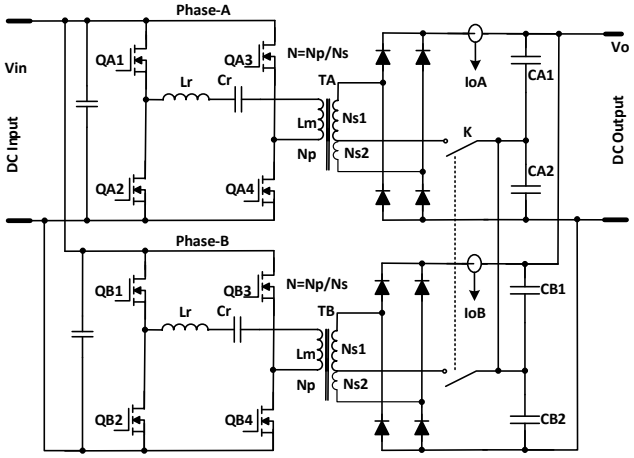


Fig.5. Gain-Switchable DC Transformer.

The DC-X uses two interleaved LLC converters with 90°phase offset. The difference from regular LLC design is that this DC-X's transformer magnetizing inductance Lm is much larger than resonant inductance Lr. The circuit quality factor Q is selected at a relatively smaller value so the converter's impedance can be less sensitive to component value variation.

For the low output voltage range (Vo< 500V), the relay K is open. The transformers' secondary outputs are rectified directly and applied to the output filter. If the battery pack voltage is detected to be in high voltage range, the relay is closed before the converters start operating. The output rectifier circuit then becomes a voltage doubler to provide a higher voltage to charge the battery pack. To meet the gain requirement on Fig. 4, the transformers' turn ratio is selected as Np:Ns1:Ns2 = 7:3:1. When the relay is open, the DC-X gain is 7: 4; when the relay is closed, then the gain becomes 7: 6. Note since Ns1 > Ns2, N1's output is doubled while Ns2 winding output terminal becomes floating when the relay is closed.

LLC converters inherently have current sharing difficulties when they are paralleled directly[19,20]. Component parameter tolerance leads to the variation of the converters' resonant frequencies and so their impedances and gains. Varying switching frequency to force their current sharing is not an option for LLC converters, due to the beat frequency problem and the periodical output current ripple issue. Interleaved LLC converters need to operate at the same frequency with 90°phase offset in order to reduce their total current ripple. Full-bridge LLC converters have the privilege to adjust their DC gain by using phase-shifting control [19,20]. For the ideal case, both full-bridge LLC converters operate with 180° phase shifting. Their average output currents are sensed and compared. If any current difference is detected, a control loop reduces the phase-shifting angle of the full bridge with higher output current. The control scheme was simulated and found to be valid. The simulation was conducted with one phase resonant inductance 10% higher than the ideal value and the other 10% lower, the control was able to adjust phase-shifting angle to achieve a good current sharing.

Fig. 6 shows the control signal diagram of the module design and Fig. 7 is the loop control diagram.

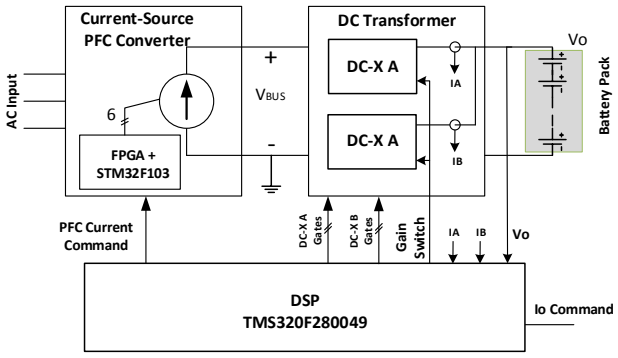


Fig. 6. Signal diagram of AD/DC module.

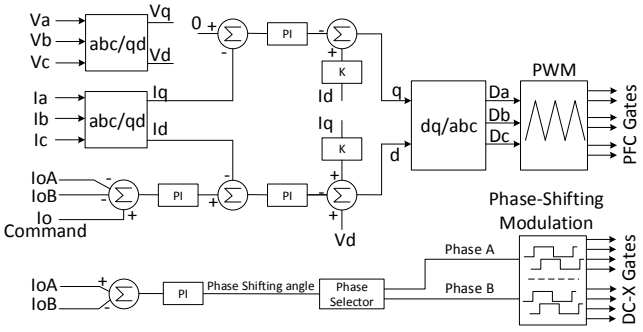


Fig. 7. Loop control diagram.

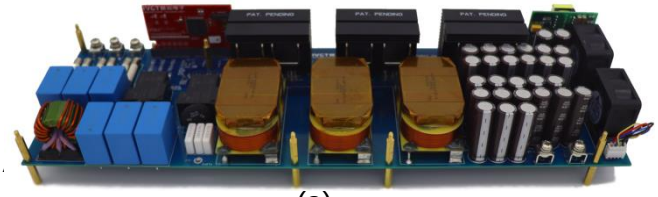
The three-phase current-source PFC is controlled by a FPGA and ST micro-controller combo circuit. The Park and Clarke transformation is

implemented with the FPGA. The DC-Xs and PFC current command are controlled by a TI DSP.

4. Experiment

To validate and benchmark this proposed new power architecture, a 20kW prototype was designed. Existing 20kW product standard size is 3U x 5U x 9U. This design aims to double the power density while reducing material and labor cost. The prototype height is reduced to 1.5U while keeping the same width and length. The current products use two PCB board structure. One board is for PFC and the other is for DC/DC converter circuitry. Each board is 1.5U high. The two boards are connected by a cable and fit into a 3U box. The new structure would enable single-board solution and simplify product assembly.

To facilitate debug and lab test, instead of using a single 5U x 9U PCB board, two 2.5U x 9U PCB boards are used. Fig. 8 shows the PFC board and DC/DC converter board.



(a)

(b)

Fig.8. (a) 20kW three-phase PFC prototype, and (b) 20kW LLC converter prototype.

The PFC board was designed with space left for bulk capacitors, so the board can be tested in either voltage mode or current mode. Each PFC switch position uses two 50mOhm 1200V TO-247-4 (IV1Q12050T4) in parallel and each LLC position uses one 50mOhm 1200V TO-247-3 (IV1Q12050T3). Both stages use SiC MOSFET drivers (IVCR1401). The rectifier circuit uses 30A/1200V SiC diodes (IV1D12030T3). The PFC and DC-X operate at 65kHz and 180kHz respectively.

Fig.9a and b show interleaved LLC converter current sharing waveforms. A large current imbalance was created deliberately by increasing one phase resonant inductance by around 15%, which resulted in 3.4A and 8.6A unbalanced output currents. After phase-shifted current sharing was enabled, both phases output 6.1A.

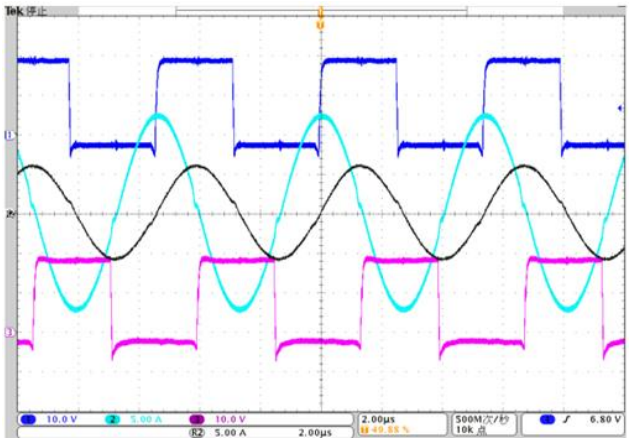


Fig. 9a.

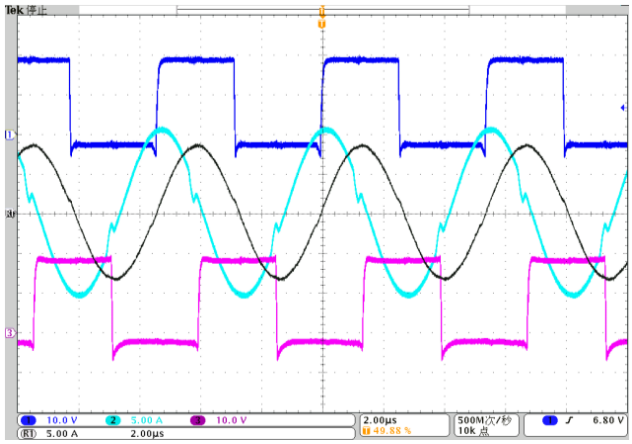


Fig. 9b.

Fig.9. LLC resonant current waveforms (a) Current sharing disable, (b) Current sharing enabled.
Channels 1 and 3: phase A and B's gate signals.
Channels 2 and 4: phase A and B's primary currents.

Note since the two full-bridge LLC converters operate at different phase shifting angles, the primary current amplitudes may be the same even though their output DC currents are equal.

Fig.10 is the system test setup and shows signal measurement positions. The PFC had 28 x 68uF/450V electrolytic capacitors, denoted by C_{PFC}, installed initially at its output. The capacitors

are divided into 14 groups. Each group has two connected in series to handle up to 900V bus voltage. The DC-X input has 2x12uF/1000V film capacitors and the output has 4 x (30uF+220uF)/ 450V film and electrolytic capacitors. A 20x2x330uF/450V capacitor bank is connected in parallel with the load to emulate a high-voltage battery pack. The test shows that the capacitor bank's reflected capacitance at the DC-X input, namely PFC output, is able to hold the PFC and system stable with reduced or even completely eliminated PFC output capacitors C_{PFC}. Fig.11 is a 10kW test result with C_{PFC} reduced by 72%. The waveforms show no notable line-frequency harmonic voltage or current ripples. However, switching-frequency voltage ripples does exist, which indicates that some minimum capacitance C_{PFC} still needed in order to keep the ripple to a desired value. To limit the PFC output voltage overshoot in case of the DC-X shutdown at heavy loads or overcurrent fault, minimum C_{PFC} value is also needed to absorb the PFC inductive energy.

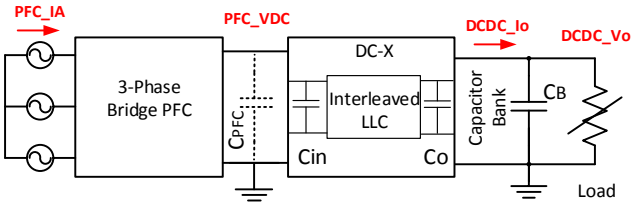


Fig. 10. PFC and DC-X system test setup.

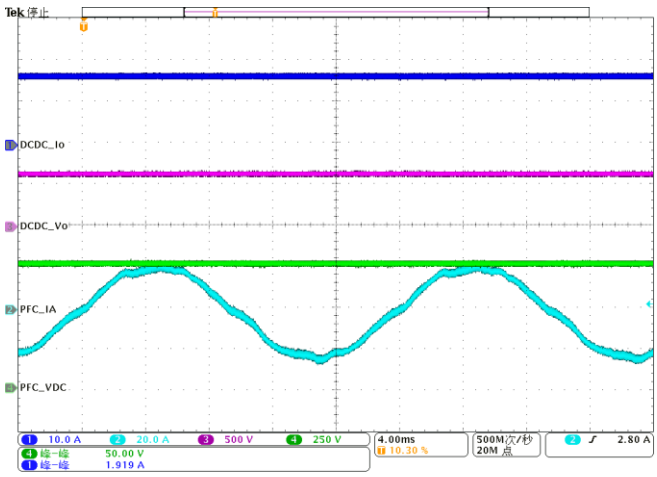


Fig.11. System key waveforms at 10kW.

Fig. 12 shows efficiency curves of each stage and the total efficiency at 400Vac input. The LLC converter stage efficiency was measured at 435V (with the relay open) and 655V (with the relay closed) outputs, which corresponded to 750V LLC input. The efficiency curves almost match each other at the two different output voltages, which indicates the topology is suitable for constant power operation.

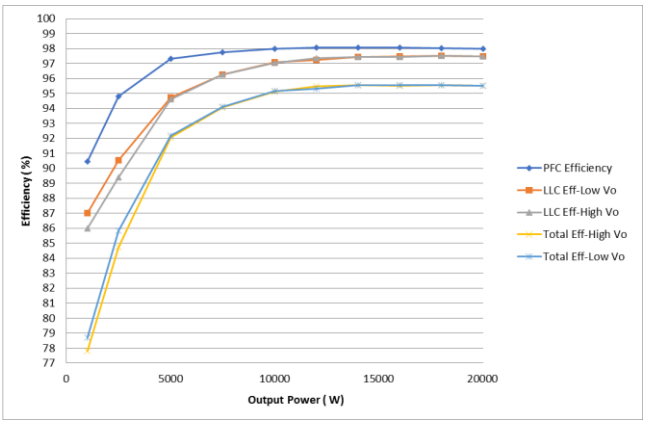


Fig.12. Power stage and system efficiencies including 20W bias loss.

Table-1 shows the comparison of this prototype and two existing products on main parameters.

Table-1: Design comparison summary

	Product A	Product B	Inventchip Prototype
Size	2Ux5Ux9U	2Ux5Ux9U	1Ux5Ux9U
Power	20kW	20kW	20kW
Topologies	Vienna + 3-Level Phase-shifted full bridge	Vienna + Series-Connected 3-phase LLC	3-phase PWM PFC+ 2-Level Interleaved LLC
PFC fs DC/Dc fs	20kHz 70kHz	24kHz fr: 107kHz 75 – 350kHz	65kHz 180kHz
Constant Power	No (constant current)	Yes	Yes
Power Devices	SiC diodes + Si MOSFETs +FRDs	SiC diodes + Si MOSFETs +FRDs	SiC MOSFETs + SiC Diodes
Efficiency	95.5% Peak 95.0% Full Load	96% Peak 95.3% Full Load	95.5% Peak and full load

Compared with the existing products, this prototype doubled the power density at a mediated efficiency. The test data were taken from the first-round-built prototype with conventional SPWM PFC control. There should be some room to fine tune the design and the control to achieve a better efficiency. The

prototype has not been evaluated at elevated temperature. However, the initial test results show promising of this power architecture.

4. Conclusions

A new power architecture has been proposed and evaluated. By using a current-source PFC and DC transformer, the PFC output bulk capacitors can be reduced or eliminated for battery charging applications. It is an important step to increase the charger module density. Utilizing wide-bandgap 1200V SiC MOSFETs, the converters can operate at higher voltage and switching frequency with simpler topologies. It is another factor to make high-density designs possible. The performance of the 20kW prototype is benchmarked with existing products. The results show good promise for this new power architecture in high density charger pile module design.

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