IVCR1401 Application Note AN-0001

The IVCR1401 is a high-speed 4A sink and source SiC MOSFET and IGBT driver. It is the first industrial SiC MOSFET and IGBT driver which includes negative voltage generation, desaturation and programmable UVLO in an 8-pin package. It is designed for low-side drive, but with a bootstrap circuit or isolated bias, it is well suitable for high-side drive as well. To reduce overcurrent responding time and improve noise immunity for SiC MOSFET applications, the driver design is enhanced, compared with an IGBT driver. Desaturation current source is increased to 1mA so a larger blanking capacitor can be used to reduce parasitic and noise impact. Most SiC MOSFETs don't have an anti-parallel diode, which results in a higher V_{SD} (body diode forward voltage) drop and makes it more difficult to use bootstrap circuit. This document will detail the solutions of SIC MOSFET gate drive with IVCR1401.

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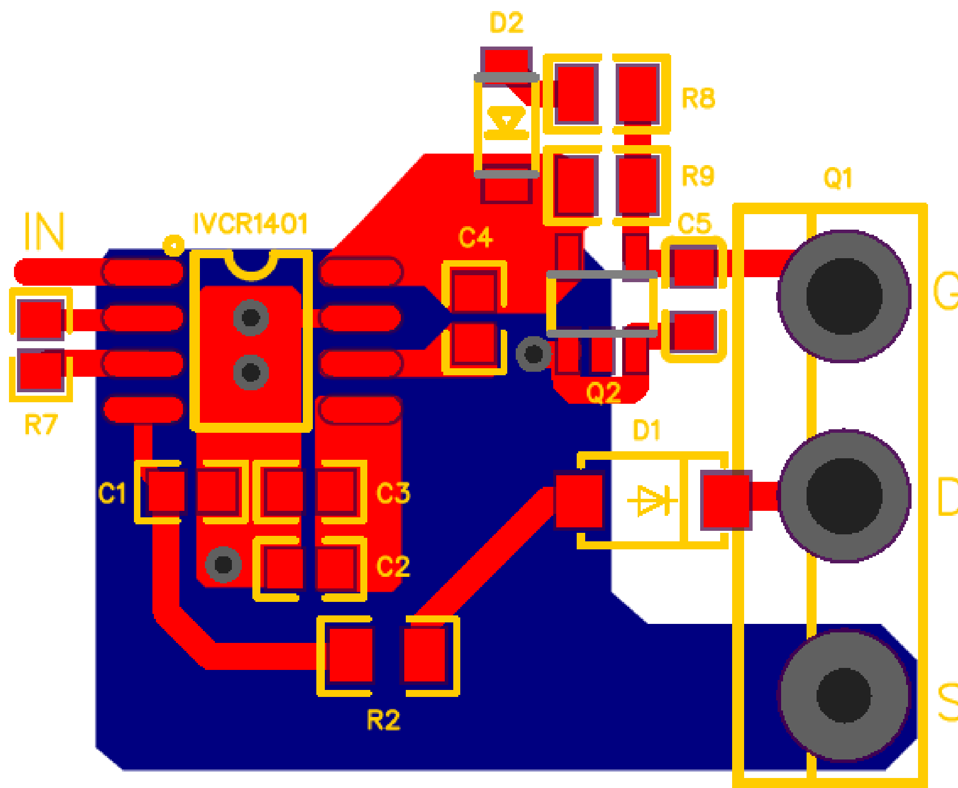
1 PCB Layout Recommendation

A good layout is a key step to achieve desired circuit performance. Solid ground is the first thing to start with. It is recommended to tie the exposed pad to the driver ground. It is a general rule that capacitors have a higher priority than resistors for location arrangement. A 1uF and a 0.1uF decoupling capacitors should be close to VCC pin and grounded to the driver circuit's ground plane. Negative voltage capacitor should locate near to OUT and NEG pins. To minimize the negative voltage ripple, a X7R capacitor with over 100 times Cg capacitance should be used. Blanking capacitor should be close to the DESAT pin of the driver as well and the capacitor should be made of C0G or equivalent materials. A small filter (with10ns time constant) may be needed at the input of IN if the input signal traces have to pass through some noisy area. Following is a recommended layout with the corresponding schematic.



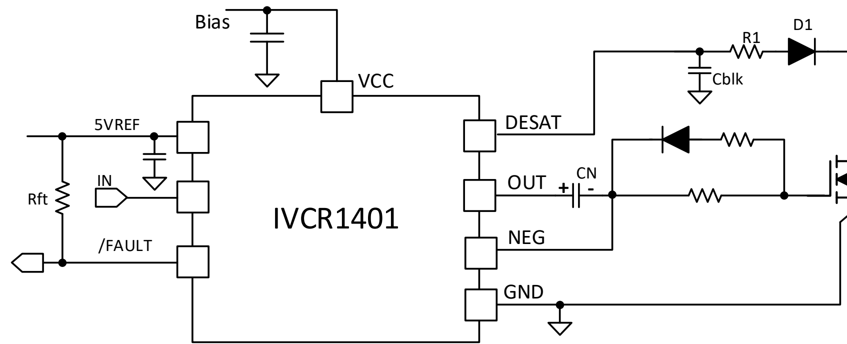
Layout Example of IVCR1401 Gate Driver Circuit

2 Vcc Selection and UVLO Programming

IVCR1401 integrates a 3.5V negative bias generation circuit. It inserts the 3.5V between the driver IC output, OUT and the power device gate or base input. Therefore, the power device's positive and negative gate drive voltages are Vcc-3.5V and -3.5V respectively. To select a proper Vcc value, circuit designers need to determine what nominal positive gate voltage is and then add 3.5V on the top of it to get Vcc voltage value. Vcc voltage monitor circuit senses Vcc, not the gate voltage, for UVLO protection. The UVLO threshold voltage is programmable. /FAULT is an open-collector output. A pull-up resistor Rft must be connected between /FAULT and 5VREF, and the different thresholds of UVLO can be selected per following suggested resistance values.

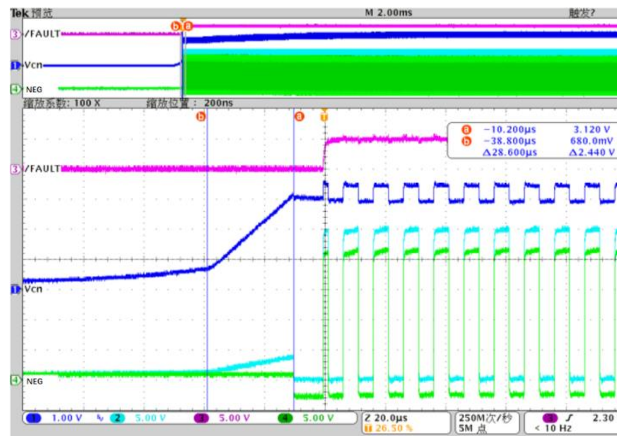
UVLO		Programming Resistance Rft	Vcc			Vg (V_{NEG})			Unit
			Min Max		Typ	Min Max		Typ	
V_{ON} V_{OFF}	Under voltage thresholds	1.3kΩ		18 17			14.5 13.5		V
		6kΩ	13.8	15.8 14.8	16.8	10.3	12.3 11.3	13.3	
		20kΩ		13.9 13.1			10.4 9.6		

The circuit connection is shown in the figure below.



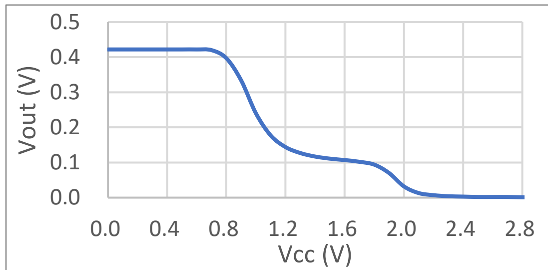
3 Voltage Buildup and Capacitor Selection

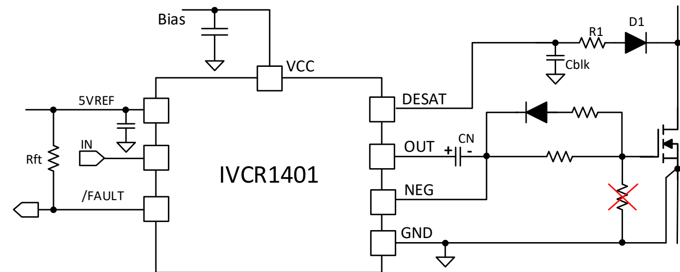
It is important for a power system to have stable biases before starting power conversion. To ensure all power switches stay at off state at power up, a negative bias needs to be built up as soon as possible. IVCR1401 has an internal current source to charge up the negative bias capacitor within tens of microseconds, depending on the capacitance. For most MOSFETs with gate capacitance less than 20nF, a 1uF capacitor would be sufficient for the gate driver circuit to build up a stable negative bias. It takes about 28us for a 1uF capacitor to be charged up. Low ESR and ESL capacitors with low variation materials, e.g. X7R, should be used. A larger capacitance can be used if lower voltage ripple across the negative bias capacitor is required. Following figure shows the negative voltage buildup at power on.



After the negative voltage is built up, the negative voltage is regulated at -3.5V by a low current (about 200 micro Amperes) charge pump. For some traditional bipolar gate drive circuit design, to avoid charge building up at a power switch gate due to Miller effect or static charge, a pull-down resistor is sometimes used. However, since IVCR1401 uses MOSFET totem-pole output, the gate is clamped to Vcc through the totem-pole's high-side MOSFETs' body diode. The driver leakage acts as a bleeding resistor to prevent charger buildup at the gate. The OUT is clamped below 0.42V at 1mA pull-up current. At power up, as soon as Vcc rises to 1.2 volts, the driver starts to pull OUT even lower,

as shown below. Any external gate pull-down resistor (Rpd) is not necessary and should not be used. Adding a pull-down resistor could result in the negative voltage moving away from -3.5V under different PWM duty cycles.





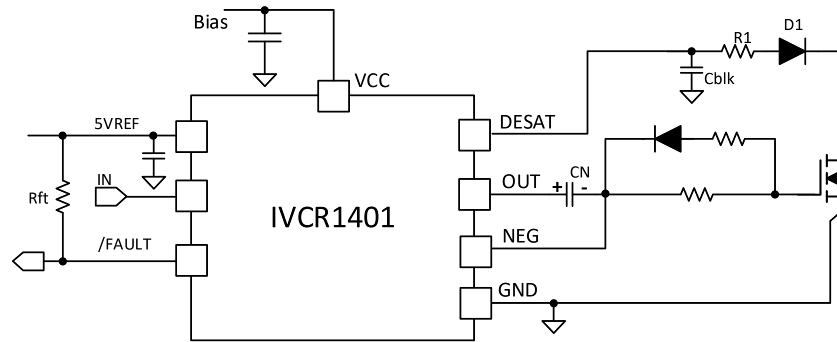
4 Desaturation Overcurrent Protection Setting

A power system usually has an accurate overcurrent protection with on-line current sensors. Desaturation (Desat) overcurrent protection should be deemed a second level protection. Under some special fault situations, e.g. bridge shoot through and inverter output terminal-to-terminal or terminal-to-ground short circuit before a filter, the on-line current sensors are not able to detect the faults, the desaturation overcurrent protection becomes a crucial and the last defense line to protect the power devices. Therefore, Desat overcurrent protection is primarily for short circuit protection. Due to large variation of Vds or Vce of a power switch device, the over current protection is a coarse protection. The over current protection threshold should be set at a conservative value to avoid premature trigger.

4.1 Over Current and Short Circuit Protection Setting

Most SiC MOSFET datasheets provide “Maximum Drain Pulse Current”. The current is usually defined as maximum allowed drain current with 10us pulse width and 1% duty cycle. The current is about 3 to 4 times of the device rated continuous current at 125°C. Over current threshold, $I_{_OCP}$ should be selected between the rated continuous current and the maximum drain pulse current. 125°C or 150°C R_{DS_ON} should be used for OCP threshold calculation.

High voltage blocking diode’s forward voltage varies with junction temperature and conduction current. The conduction current is the 1mA constant current sourcing from IVCR1401 DESAT pin. A PiN diode has a negative temperature coefficient. For conservative calculation, 25°C diode forward voltage can be used for the OCP threshold calculation.



For current limit setting, the following equation can be used,

$I_{limit} = (V_{th} – R1^{*} I_{DESAT} – V_{F_D1})/ R_{ds_on}$

where R1 is a programming resistor, V_{F_D1} is high voltage diode forward voltage, R_{ds_on} is SiC MOSFET turn-on resistance at estimated junction temperature, such as 150°C, V_{th} is 9.5V and I_{DESAT} is 1mA.

When short circuit or over current happens, the power device's (SiC MOSFET or IGBT) drain or collector current can increase to such a high value that the devices get out of saturation state, and Vds or Vce of the device will rise to a substantially high value (>>9.5V). DESAT pin with a blanking capacitor Cblk, normally clamped to Id x Rds_on, now is able to charge up much higher by an internal 1mA constant current source. When the voltage reaches typical 9.5V threshold, OUT and /FAULT are both pulled low. A 200ns blank time is inserted at OUT rising edge to prevent DESAT protect circuit from being triggered prematurely due to Coss discharge. By selecting different capacitance, turn-off delay time (external blanking time) can be programmed. The blanking time can be calculated with,

$T_{eblk} = C_{blk} \cdot V_{th} / I_{DESAT}$

For example, if C_{blk} is 47pF, T_{eblk} = 47pF ·9.5V / 1mA = 446ns.

Note T_{eblk} includes internal T_{blk} 200ns blanking time already.

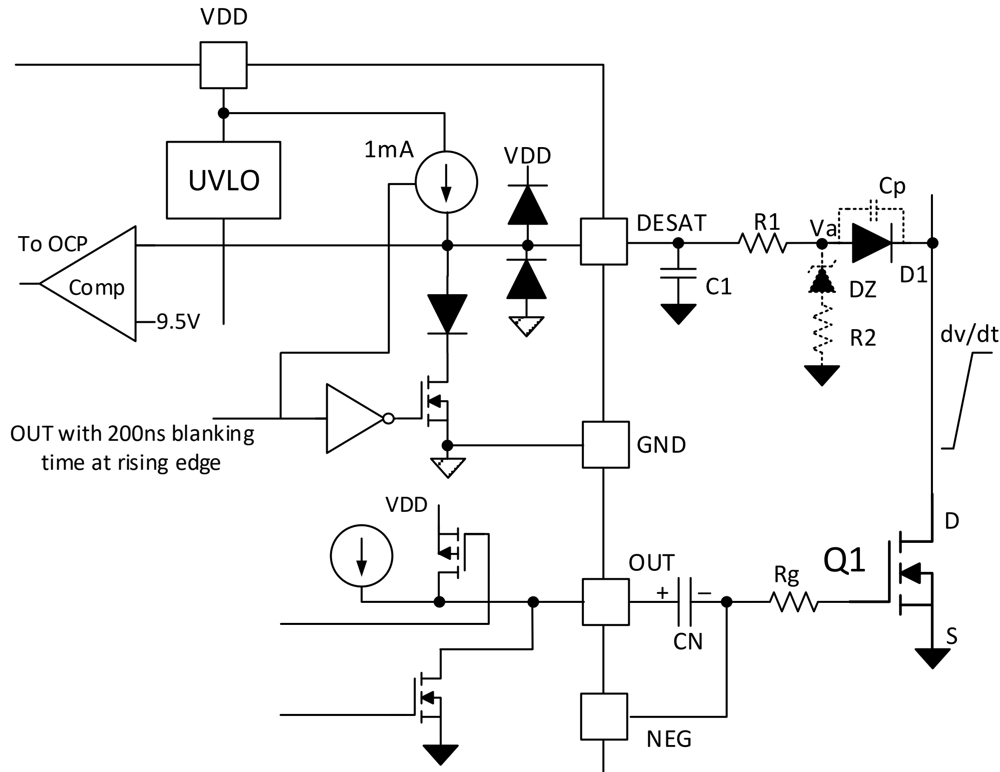
A different power system usually requires a different turn-off time. An optimized turn-off time can maximize the system short circuit capability while limiting Vds and bus voltage ringing.

4.2 dv/dt Impact on Short Circuit Turn-Off Delay

High voltage blocking diode D1 always has some parasitic capacitance. Voltage coupling by the parasitic capacitance Cp at high dv/dt of Vds can rise or push down the diode's anode voltage Va considerably. The large voltage variation of Va can in turn charge or discharge the blanking capacitor C1 to an unexpected value and cause false trigger or long delay of OCP. This issue becomes more significant due to high switching

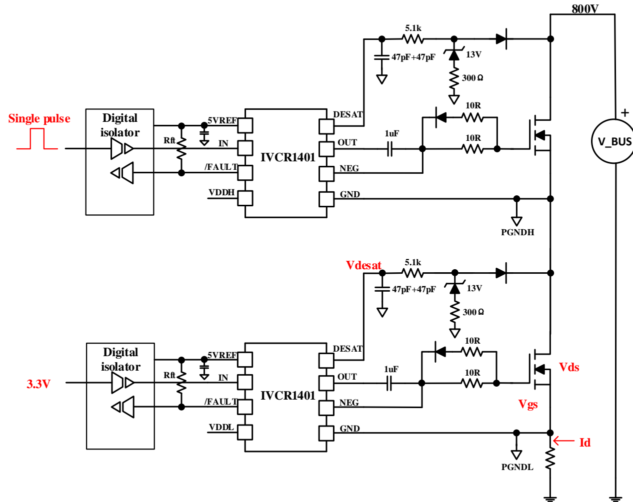
speed of SiC MOSFET. To clamp the voltage rising level, a 12V Zener diode is recommended. The Zener also limits the negative voltage of Va.

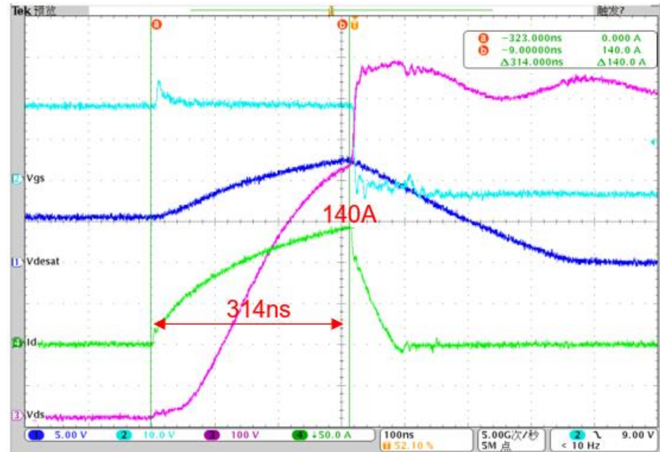
One special attention needed to pay here is that most SiC MOSFETs don't have an anti-parallel diode. SiC MOSFET's body diodes usually have 3 to 5 voltage forward voltage drop, which is higher than the combined voltage drop of D1 and DZ. To prevent the main current from passing through D1 and DZ, a few-hundreds Ω resistor is recommended to connect in series with DZ. To minimize the impact of Cp, it is strongly recommended to use a low capacitance diode for the voltage blocking purpose.



There are two main half-bridge short circuit cases. One case is turning on one power switch with the other power switch already on. The other case is turning on one power switch with the other one shorted.

For the first case (Case one), as shown below, since bottom MOSFET is already on, DESAT is charged to a steady state voltage, which is around 5V in the following example. With top MOSFET turning on, shoot through current increasing and Vds of bottom MOSFET rapidly rising, voltage of DESAT rises quickly and reaches desaturation threshold in 314ns.

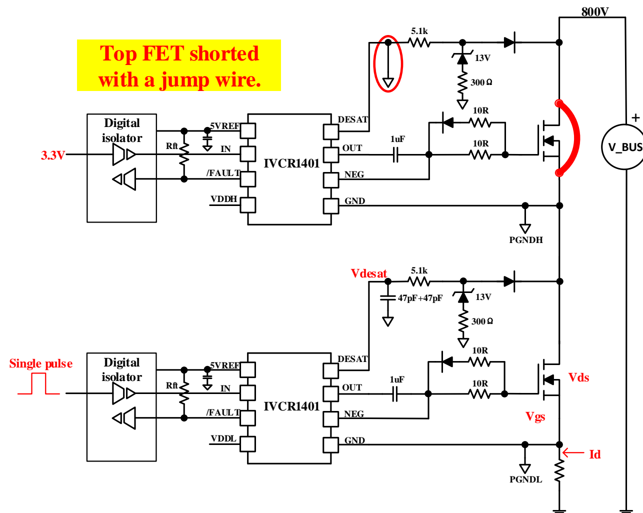


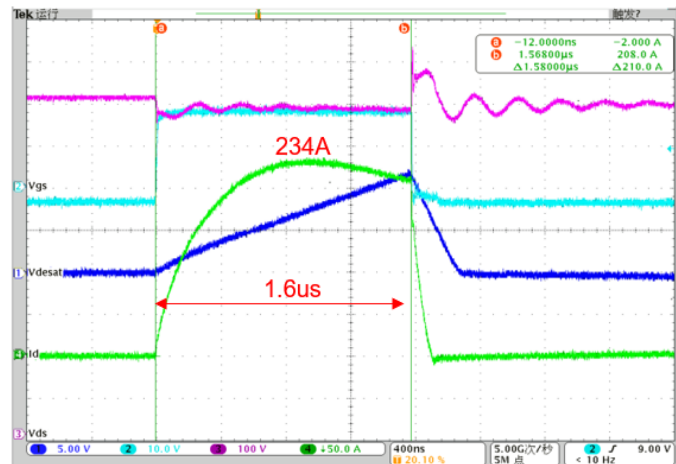


Note: all four channels are low side signals.

Case one: Turning on one power switch with the other power switch already on

For the second case, since top MOSFET is already hard shorted with a jump wire, no high dv/dt impact exists. The bottom MOSFET turn-on delay totally relies on blanking capacitance. The capacitor is charged linearly from zero volts and desaturation protection is triggered at 1.6us, which is much longer than the delay time of the first case.





Note: all four channels are low side signals.

Case Two: Turning on one power switch with the other power switch shorted

If the top MOSFET stays on with desaturation protection disabled, due to Vds (of the bottom MOSFET) swinging down rapidly, it discharges the bottom driver's blanking capacitor partially and prolongs the desaturation protection delay time to 1.8us.

Note: all four channels are low side signals.

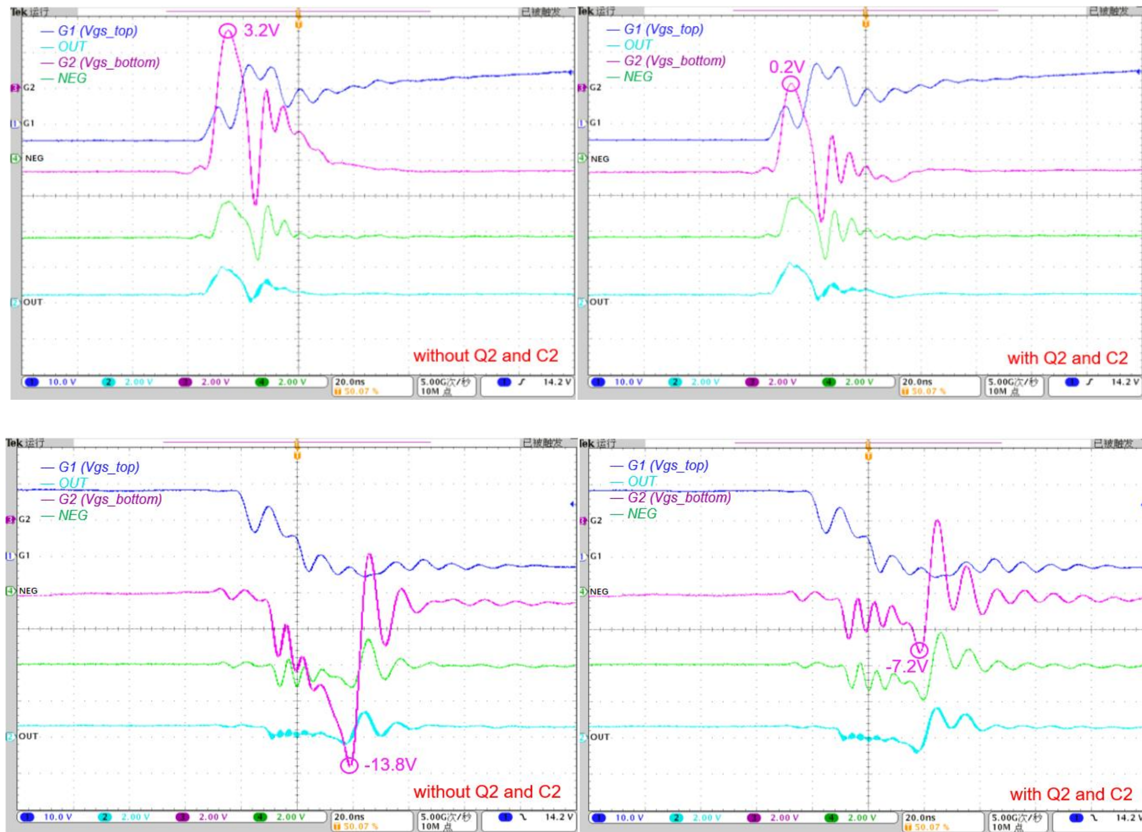
Turning on one power switch with the other power switch on and Desat disabled

These tests indicate that to have a stable and fast short circuit protection, both top-side and bottom-side drivers should have desaturation protection enabled.

5 High-Side Drive with Bootstrap Circuit

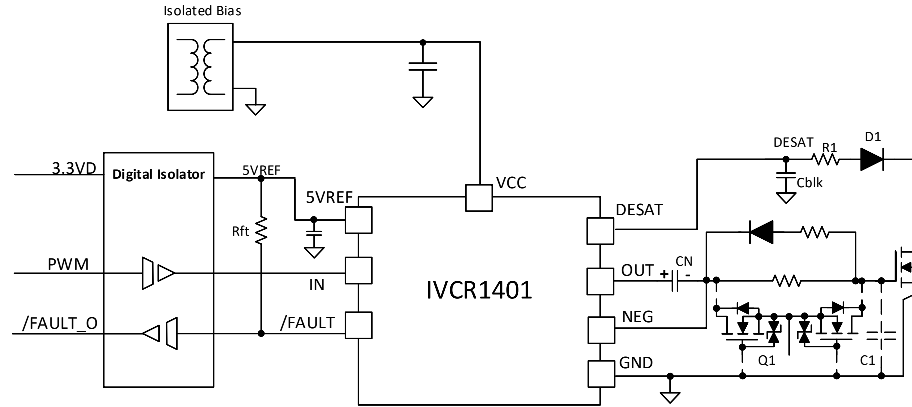
For compact and low cost design, bootstrap is preferred. However, it is difficult to generate a negative bias with bootstrap circuit, due to grounding issues. IVCR1401 generate a negative bias at the driver output, not a voltage below driver IC ground. This unique approach solves the grounding issue and makes it possible for a bootstrapped power to generate a negative bias. Q1, C1, Q2 and C2， which form a local Miller clamp circuit, are reserved for reducing voltage spike produced by Miller effect at a high dv/dt rate if needed. Following circuit diagram shows the circuit configuration.

Following figures show the comparison of positive and negative voltage spike produced by Miller effect with and without Q2, C2. Channel 2 (OUT signal) and Channel 4 (NEG signal) are bottom-side signals. Both positive and negative voltage spike can be reduced greatly after adding proper Q2 and C2.



6 High-Side Drive with Isolated Bias

Due to both circuit topology and operation condition limitations, an isolated bias is required for reliable gate drive design. The solution is straight forward, as shown in the following figure.



Isolated Bias
3.3VD
Digital Isolator
5VREF
Rft
5VREF
VCC
PWM
IN
/FAULT_O
/FAULT
IVCR1401
DESAT
R1
D1
Cblk
DESAT
OUT
CN
+
-
NEG
GND
Q1
C1