IVCR2401 Application Note AN-0002

The IVCR2401 is a 4A dual-channel, high-speed, low-side gate driver, capable of effectively and safely driving MOSFETs and IGBTs. Low propagation delay and mismatch with an optional exposed pad SOIC-8 package enables MOSFETs to switch at hundreds of kHz. It is very suitable for server and telecom power supply's synchronous rectification driving, where synchronous MOSFET's dead time accuracy directly impacts converter's efficiency. The driver is capable to parallel two channels to increase output driving current. When only one enable pin is tied to high, both channel's output stages are driven by the same logic signal. This unique feature reduces two channels' mismatch significantly and makes the driver very suitable for paralleled-switch’s driving. The input thresholds are based on TTL with voltage tolerance up to 20V.

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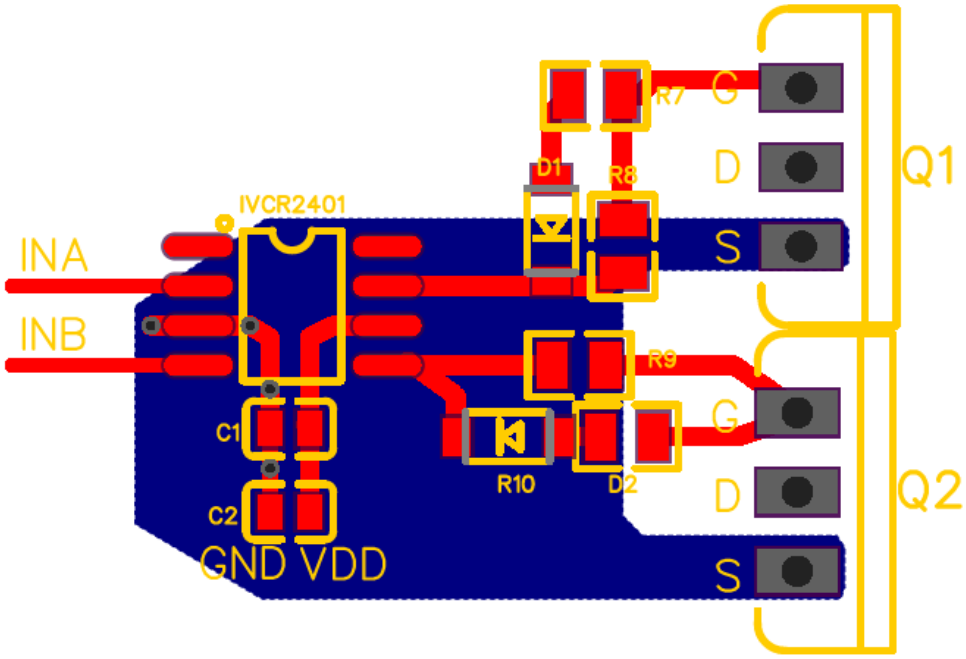
1 PCB Layout Recommendation

A good layout is a key step to achieve desired circuit performance. Solid ground is the first thing to start with. It is recommended to tie the exposed pad to the driver ground. It is a general rule that capacitors have a higher priority than resistors for location arrangement. A 1uF and a 0.1uF decoupling capacitors should be close to VDD pin and grounded to the driver circuit’s ground plane. Following is a recommended layout with the corresponding schematic.

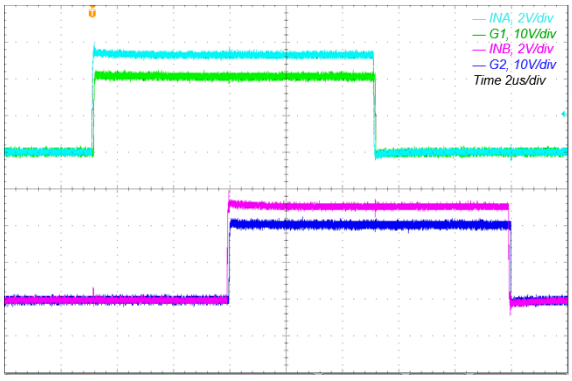


Layout Example of IVCR2401 Gate Driver Circuit

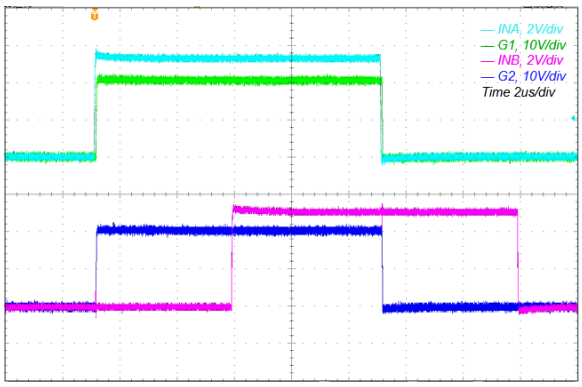
2 Synchronous Function

When only one Enable pin is tied to high, both channel's output stages are driven by the same logic signal. This unique feature reduces channels' mismatching significantly and makes the driver very suitable for paralleled switches' driving. The following three configurations and tests demonstrate this feature.

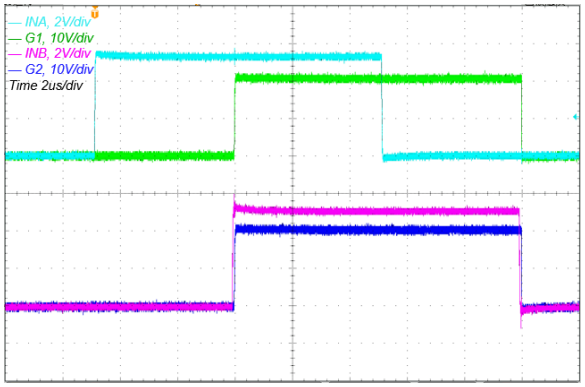
When ENA and ENB are floating and the input signal INB delays INA by 5us, the output signal G1 follows INA and G2 follows INB, as shown in the following. When ENA is connected to a high-level logic and ENB is left floating, both outputs G1 and G2 follow INA. When ENB is connected to a high-level logic and ENA is left floating, both output signals G1 and G2 are follow INB.



ENA and ENB both floating



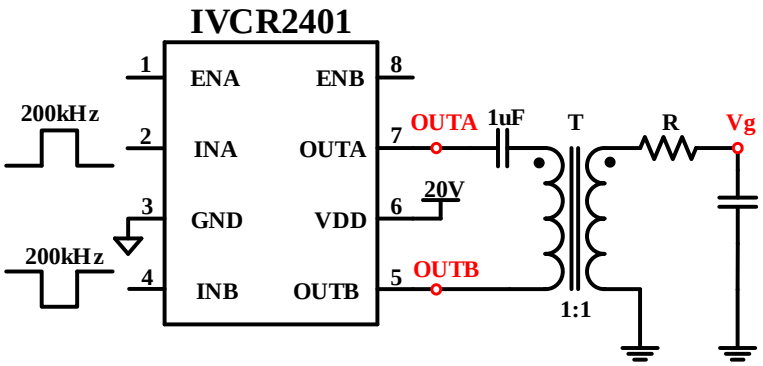
ENA tied to a high logic level and ENB floating



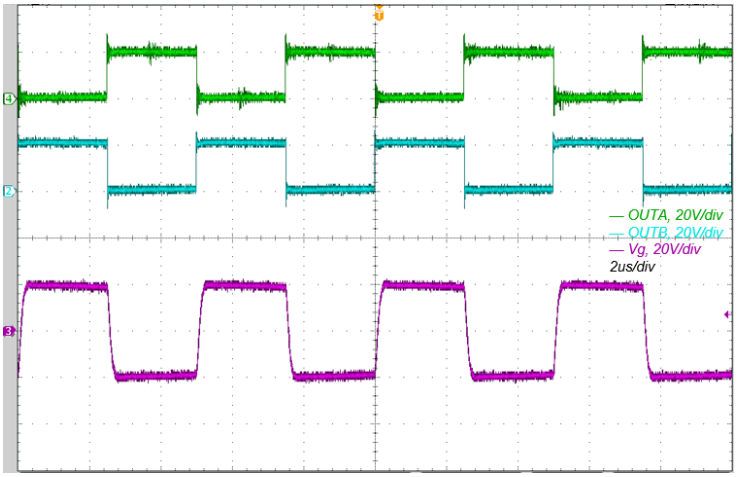
ENB tied to a high logic level and ENA floating

3 Isolated Gate Drive

IVCR2401 can be used for an isolated gate driving circuit. The following simple circuit is employed to demonstrate the application. The input signals of INA and INB are 200kHz square waves and 180 degrees out of phase. The outputs OUTA and OUTB drive an isolated transformer's primary side through a 1uF DC blocking capacitor. The transformer's secondary drives a capacitor, which emulates a MOSFET's gate capacitance. R is a gate drive resistance. The gate signal waveform Vg is shown in the following scope snap shot. The Vg is a symmetrical waveform with amplitudes changing between +20V and -20V. The driving scheme is suitable for Si IGBT and MOSFET drive.



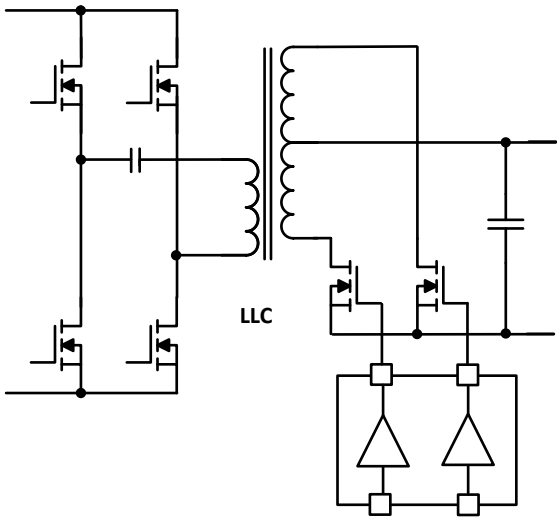
Isolated gate driving circuit



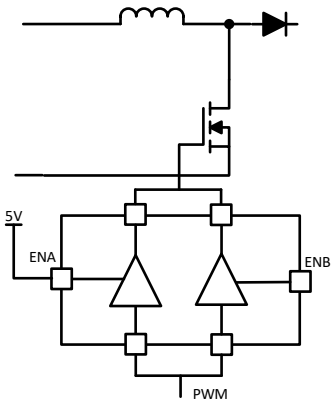
The output of the Isolated gate driving circuit

4 Non-isolated Gate Drive Applications

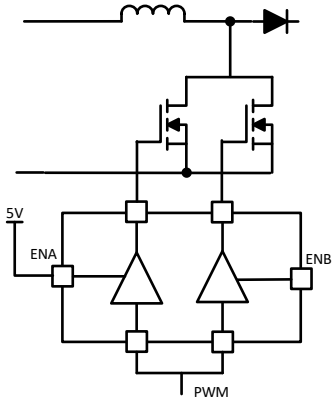
The following circuit diagrams show three common non-isolated gate drive implementation cases. The first one is synchronous rectification MOSFET drive. It can be found in a LLC converter with low-voltage output, such as 12V, where two synchronous MOSFETs are driven by IVCR2401's two channels separately. The second case is to drive a large MOSFET or a module, whose gate capacitance is significant and requires a large drive current. For the case, only one enable pin (ENA or ENB) is tied to high, both channel's output stages are then driven by the same logic signal, and the outputs can be paralleled directly to drive a large device. When the two outputs drive two MOSFETs separately instead, this is the third case, as shown in the third figure below. The two MOSFET are driven simultaneously with the same input logic to achieve better current sharing. Both the second and the third cases benefit from the IVCR2401's unique feature of extra small mismatching between the output channels.



Two channels driven separately



Two paralleled switches driven by a large switch driven by two paralleled



Two outputs with minimized mismatch outputs