IVCR1401 EVM User's Guide

This user's guide describes the IVCR1401 evaluation module (EVM), providing necessary information for the driver test setup and performance evaluation. This document contains the EVM schematic, bill of materials (BOM), assembly drawing and board layouts.

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1 Introduction

The IVCR1401 EVM is a 4A single-channel, high-speed smart driver evaluation module that provides a test platform for a quick and easy startup and feature evaluation of the IVCR1401 driver. It is powered by a single 35V external supply and features programmable UVLO of VDD, negative voltage UVLO detection and desaturation detection/short-circuit protection which can be easily verified by a comprehensive set of test points and jumpers.

1.1 IVCR1401 Applications

- EV On Board Chargers
- EV/HEV inverters and charging stations
- PV boosters and inverters
- UPS
- AC/DC and DC/DC converters

2 Schematic, Bill of Materials and Layout

This section provides a detailed description of the IVCR1401 EVM schematic, bill of materials (BOM) and layout.

2.1 IVCR1401 EVM Schematic

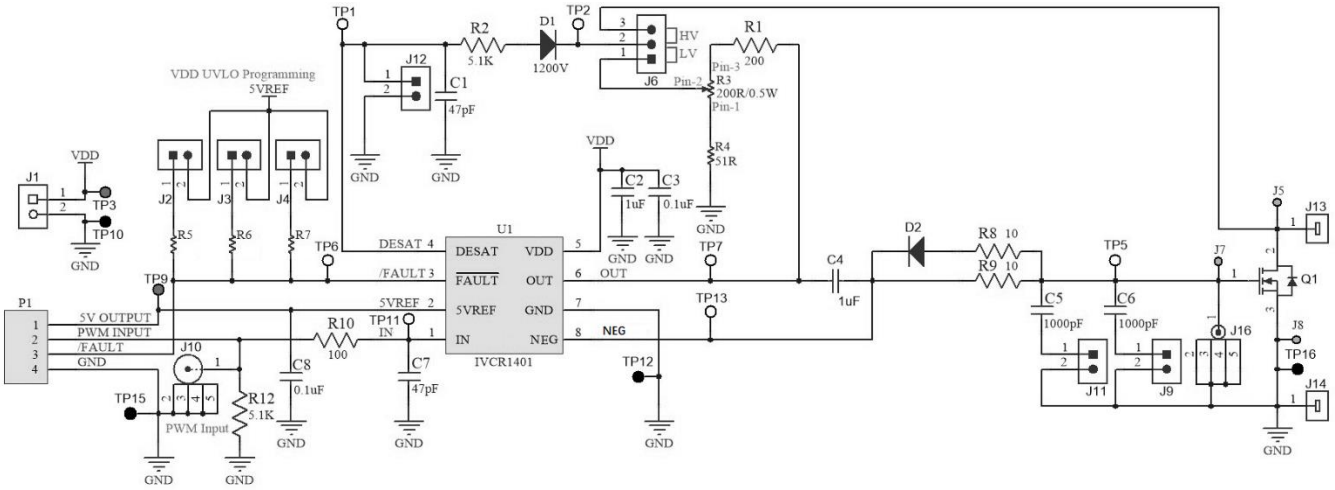

Figure 1. IVCR1401 EVM Schematic

2.2 IVCR1401 EVM Bill of Materials

Table 1. BOM

	Designator	Part Number	Description	Footprint	Quantity	DNP
1	C1, C7	0603CG470J500NT	CAP CER 47PF 50V 0603 SMD	0603	2	
2	C2, C4	GMK107BJ105KA-T	CAP CER 1UF 35V X5R 0603	0603	2	
3	C3, C8	0603B104K500NT	CAP CER 0.1UF 50V X7R 10% 0603	0603	2	
4	C5, C6	CL10B102KB8NNNC	CAP CER 1000PF 50V X74 10% 0603	0603	2	
5	D1	STTH112A	DIODE GEN PURP 1.2KV 1A SMA	SMA	1	
6	D2	MBR0540	DIODE SCHOTTKY 40V 500MA SOD123	SOD-123	1	
7	J1	KF350-2P	TERM BLK 2POS SIDE ENT 3.5MM PCB	KF350-2P	1	
8	J2, J3, J4, J9, J11, J12	5-146261-1	Header, 100mil, 2x1, Gold, TH	HDR1X2	6	
9	J5, J7, J8	0353-0-67-80-03-27-10-0	CONN PIN RCPT .040-.060 SOLDER	0353-0	3	
10	J6	TSW-103-07-G-S	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	1	
11	J10	112404	Connector, TH, BNC	Amphenol_112404	1	
12	J13, J14	74650073R	BUSH, THR OPENM3, THR 2.5MM	74650073R	2	
13	J16	PK007-015	PCB ADAPTER PACK	PK007-015	1	DNP
14	P1	5-146274-4	CONN HDR BRKWAY .100 4POS VERT	HDR1X4	1	
15	Q1	C2M0025120D	MOSFET, N-CH, 1200 V, 90 A, TO-247	TO-247	1	DNP
16	R1	RTT052000FTP	RES 200 OHM 1/8W 1% 0805	0805	1	
17	R2, R12	0805W8J0512T5E	RES 5.1K OHM 1/4W 5% 0805	0805	2	
18	R3	3362P-201	TRIMMER 200 OHM 0.5W PC PIN TOP	3362P-201	1	
19	R4	0805W8F510JT5E	RES SMD 51 OHM 1% 1/8W 0805	0805	1	
20	R5	CR0603-FX-1301ELF	RES SMD 1.3K OHM 1% 1/10W 0603	0603	1	

21	R6	M55342E12B6E00RWS	RES SMD 6K OHM 1% 1/10W 0603	0603	1	
22	R7	CR0603-FX-2002ELF	RES SMD 20K OHM 1% 1/10W 0603	0603	1	
23	R8, R9	0805W8F100JT5E	RES 10 OHM 1/8W 1% 0805 SMD	0805	2	
24	R10	RTT03101JTP	RES 100 OHM 1/10W 5% 0603	0603	1	
25	TP1, TP5, TP6, TP7, TP11, TP13	5002	Test Point, Miniature, White, TH	KEYSTONE5002	6	
26	TP2	5002	Test Point, Miniature, White, TH	KEYSTONE5002	1	DNP
27	TP9	5000	Test Point, Miniature, Red, TH	KEYSTONE5000	1	
28	TP3	5000	Test Point, Miniature, Red, TH	KEYSTONE5000	1	DNP
29	TP12, TP15, TP16	5001	Test Point, Miniature, Black, TH	KEYSTONE5001	3	
30	TP10	5001	Test Point, Miniature, Black, TH	KEYSTONE5001	1	DNP
31	U1	IVCR1401	IC GATE DVR IVCR1401 8SOIC	SOIC-8	1	

2.3 Layout and Component Placement

Figure 2 and Figure 3 top and bottom assemblies of the printed circuit board (PCB) show the component placement on the EVM.

Figure 4 and Figure 5 show the top and bottom layouts.

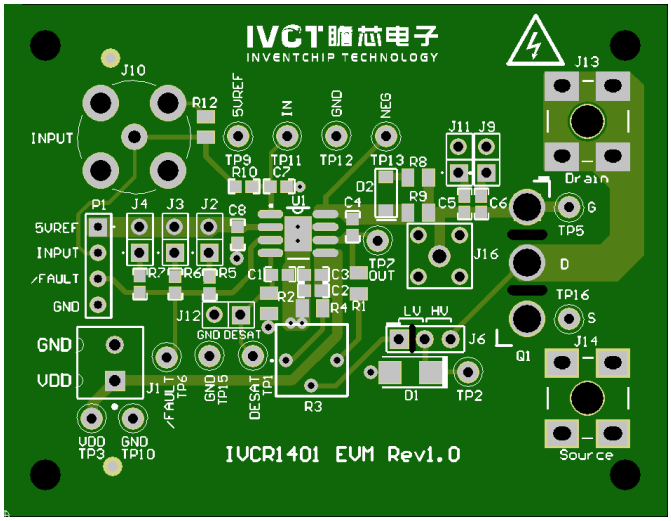

Figure 2. Component Placement — Top Assembly

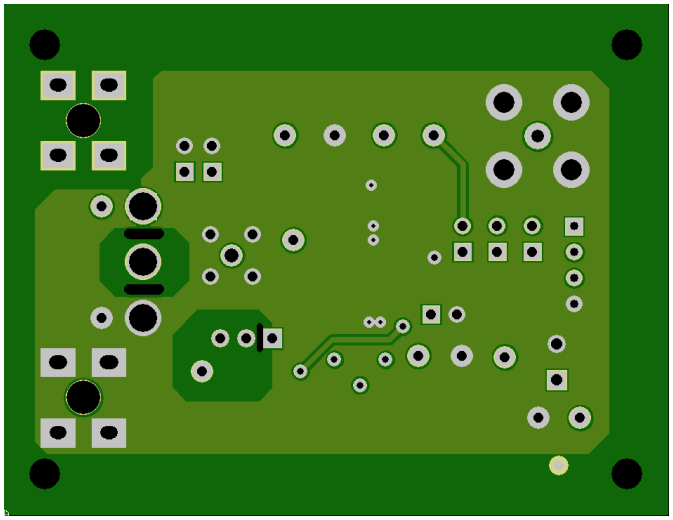

Figure 3. Component Placement — Bottom Assembly

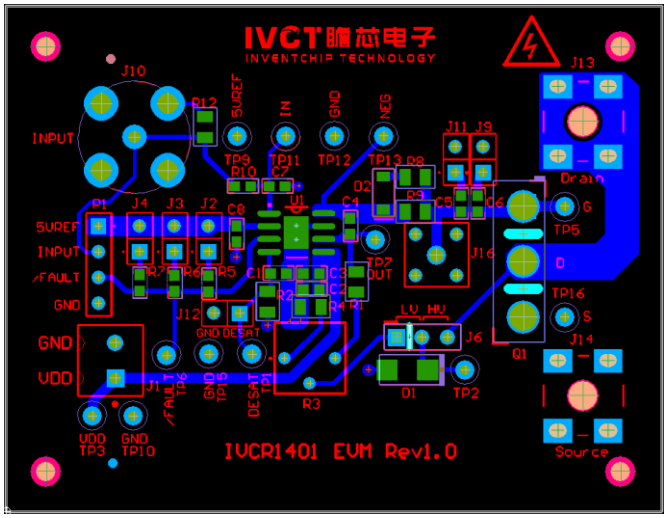

Figure 4. Layout — Top

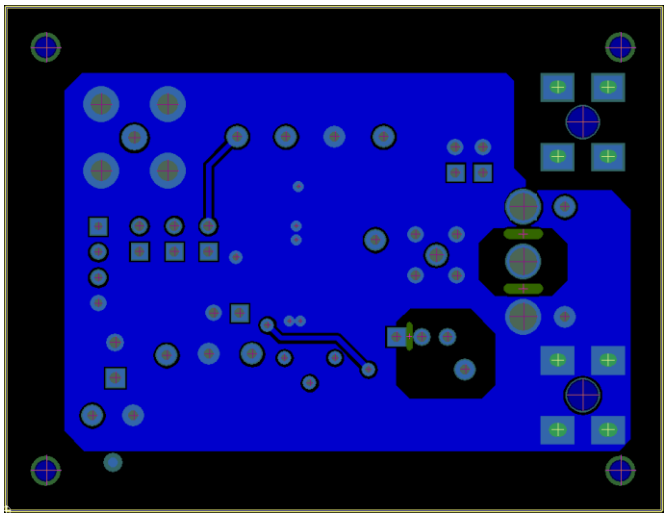

Figure 5. Layout — Bottom

3 EVM Connectors, Test Points and Jumpers

This section describes the connectors, test points and jumpers on the EVM as well as how to connect, set up and properly use the EVM.

3.1 EVM connectors

Table 2 lists the following connectors and headers on the IVCR1401 EVM.

Table 2. List of Onboard Connectors and Headers

Connectors/Headers	Silkscreen Label	Function	Description
J1	VDD, GND	Power supply	Power supply connector for the device.
J2	/	Rft=20kΩ	Connect a 20kΩ pull-up resistor between 5VREF and /FAULT to program VDD UVLO_r=13.9V, UVLO_f=13.1V
J3	/	Rft=6kΩ	Connect a 6kΩ pull-up resistor between 5VREF and /FAULT to program VDD UVLO_r=15.8V, UVLO_f=14.8V
J4	/	Rft=1.3kΩ	Connect a 1.3kΩ pull-up resistor between 5VREF and /FAULT to program VDD UVLO_r=18.0V, UVLO_f=17.0V
J6	LV, HV	Desaturation detection	If connecting LV, you can change R3 value to simulate desaturation detection when short circuit or overload happens; If connecting HV, you can use desaturation detection when doing actual short circuit experiment.
J9	/	Cload is 1000pF	Connect C6 between Q1 gate and source
J10	INPUT	Input signal	input signal from BNC connector for the device
J11	/	Cload is 1000pF	Connect C5 between Q1 gate and source
J12	GND, DESAT	Disable desaturation detection	Connecting J12 can disable desaturation detection.
J13	Drain	Q1 drain	Connected with Q1 drain
J14	Source	Q1 source	Connected with Q1 source

3.2 EVM Test Points

Table 3 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 3. Test Points

Test Point	Silkscreen Label	Function	Description
TP1	DESAT	DESAT	Connected with DESAT pin
TP2	GND	Cathode of high voltage diode	Connected with cathode of high voltage diode
TP3	VDD	Power supply	Power supply for the device
TP5	G	Q1 gate	Connected with Q1 gate
TP6	/FAULT	Fault signal	Connected with FAULT pin
TP7	OUT	OUT output signal	Connected with OUT pin
TP9	5VREF	5V reference for external circuit	Connected with 5VREF pin
TP10, TP12, TP15	GND	Ground	Connected with ground
TP11	IN	Signal input voltage	Connected with IN pin
TP13	NEG	Negative voltage output	Connected with NEG pin
TP16	S	Q1 source	Connected with Q1 source
J16	/	Q1 gate and source	Used to measure Vgs

3.3 EVM Jumpers

Table 4 lists the Jumpers on the IVCR1401 EVM. As ordered, the EVM has four jumpers pre-installed.

Table 4. List of Onboard Jumpers

Jumper	Default Connection	Description
J4	Rft=20kΩ	Connect a selected pull-up resistor between 5VREF and /FAULT to program VDD UVLO.
J6 (LV)	Simulate desaturation protection	Change the voltage at resistor pot R3 divider output to emulate Vds (Vce) of a power device. Vary R3 value to create short circuit or overload condition.
J9, J11	Cload is 1000pF+1000pF	Connect C6 and C5 between Q1 gate and source

4 EVM Setup and Operation

This section describes the functionality and operation of the IVCR1401 EVM.

4.1 Test Equipment

The test equipment includes:

DC Power Supply —— DC power supply capable of providing at least 35V.

High Current and Low Voltage DC Power Supply —— needed for a real short circuit test only. Voltage should be within 12V to 48V and the output current selected based on power device saturation current.

Function Generator —— Function Generator with at least two channels capable of providing 0V/5V 50kHz square wave.

Oscilloscope —— Oscilloscope with four channels of analog type capable of 100MHz or higher bandwidth with high-impedance scope probes capable of handling 50V.

Multimeter —— Digital multimeter capable of monitoring input DC voltages, or other nodes on the EVM.

4.2 Recommended Test Setup and Operating Conditions

Figure 6 shows the EVM test setup. Table 5 lists the recommended operating conditions.

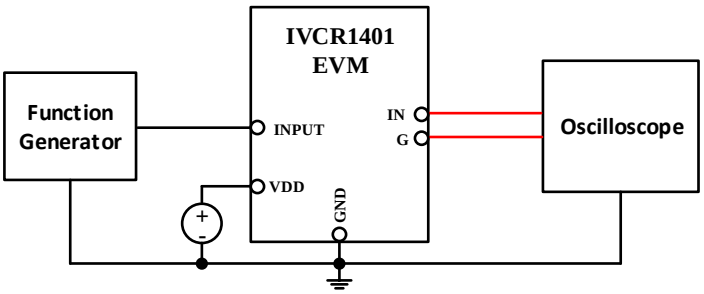

Figure 6. Recommended Test Setup

Table 5. Recommended Operating Conditions

Parameter		Min	Max	Unit
VDD	Supply voltage (Rft=20kΩ)	18	25	V
INPUT	Input voltage	0	15	V
T_A	Operating ambient temperature	25 (typical)	/	°C

4.3 EVM Setup and Power-Up Procedure

To power the EVM, follow these steps:

Step 1. Set the DC power supply current limit around 0.1A and power up the board by applying 20V to VDD.

Step 2. Connect the function generator output to INPUT (J10) and set the function generator to produce a pulse with low amplitude 0V and high amplitude 5V at desired frequency and duty cycle.

Step 3. Adjust R3 to reduce the voltage divider output, make sure the voltage is low enough and not trigger desaturation protection. OUT should have an output and DESAT pin should be charged up linearly at this point.

Step 4. Raise the divider output voltage until desaturation protection is triggered to emulate over current condition and protection.

Step 5. Use scope to capture waveforms.

5 Performance Data, Test Verification Waveforms and Typical Characteristic Curves

5.1 Propagation Delay, Rise and Fall Times

Figure 7 shows the propagation delay, rise and fall times as measured on the EVM.

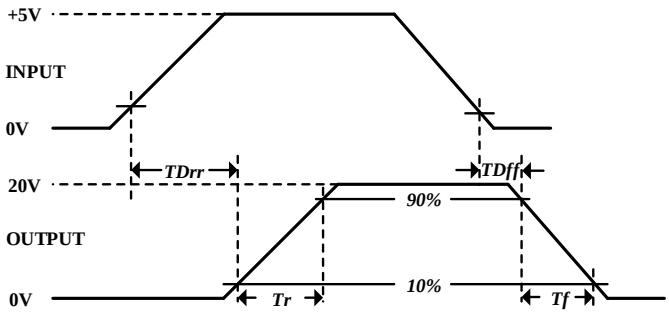

Figure 7. Switching Waveforms

The load capacitance testing condition is 2nF and VDD=20V, and the driver input signal INPUT voltage is set to 5V logic with 50kHz. Table 6 lists the EVM test results.

Table 6. EVM Test Results

Delay Time, IN Rising (IN to OUT)	Delay Time, IN Falling (IN to OUT)	Rise Time	Fall Time
56 ns	41 ns	49 ns (Rg_on=10Ω, Rg_off=5Ω)	42 ns (Rg_on=10Ω, Rg_off=5Ω)

Note: Due to gate driver resistor Rg, the rise time and fall time are longer than Datasheet values.

Figure 8 and Figure 9 show the propagation delay, rise time and fall time measurements on the EVM.

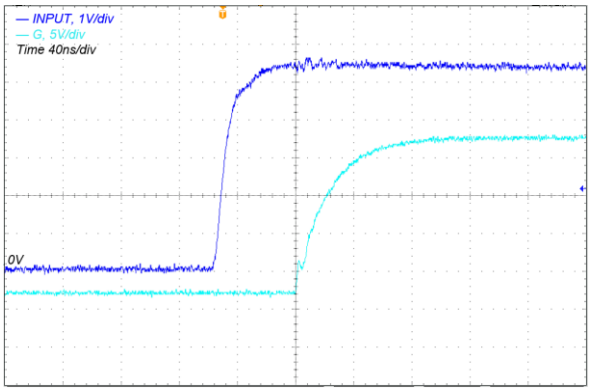

Figure 8. IVCR1401 Input Rising

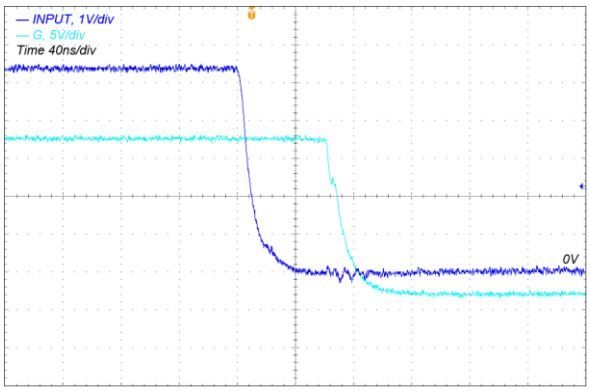

Figure 9. IVCR1401 Input Falling

5.2 DESAT Protection

IVCR1401 EVM provides two desaturation detection circuits. One is used for DESAT protection emulation without a high current and the other is used to operate at an actual

short circuit condition. Following describes the use of these two desaturation detection circuits.

a. Desaturation detection emulation circuit

Before using this desaturation detection circuit, pin 1 and pin 2 of J6 with silkscreen label LV should be shorted.

When the driver output OUT is high, the gate voltage is about VDD-3.5V. The gate voltage is then divided down by resistor pot R3 and its series connected resistors. The voltage is the emulated Vds. Blocking diode D1 blocks blanking capacitor C1 from being charged by the emulated Vds and the blanking capacitor C1 is then charged up by the driver internal 1mA current source I_{DESAT}. C1 voltage rise linearly until it is clamped by the emulated Vds or pulled to ground if overcurrent protection is triggered. Short circuit delay time can be programmed by C1.

The emulated Vds can be adjusted by the resistor pot R3. Under normal operation, Vds is not high enough to trigger desaturation protection and the blocking diode D1 conducts, which divers some current to R2 and slow down C1 charging up. R2 acts as a Vds desaturation programming resistor and a filter to reduce the impact of D1 parasitic capacitance.

When desaturation is detected, the /FAULT signal, DESAT and OUT are all pulled low. The /FAULT signal stays low for 10us, disregarding fault condition. /FAULT is an auto recovery signal. After 10us timer expires and fault condition is removed, the driver will restart. Figure 10 shows this procedure.

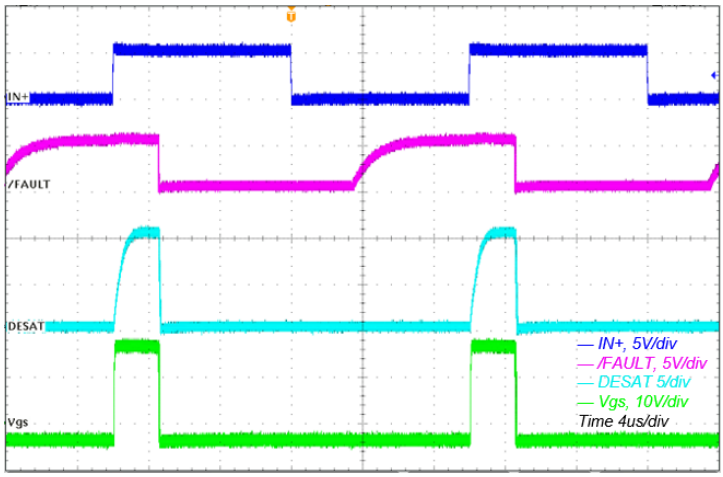

Figure 10. The procedure of desaturation is detection

b. Desaturation detection circuit for actual short circuit test

Before using this desaturation detection circuit, pin 2 and pin 3 of J6, labeled as HV, should be shorted and a power device (SiC MOSFET or IGBT to be tested) should be installed at Q1 position.

The Drain (J13) and Source (J14) are connected to a high-current voltage source, and VDD is set to make Vgs to an appropriate gate drive voltage value. A voltage pulse is then applied to the INPUT.

Note that if the power device's recommended gate-voltage is Vg, VDD should be Vg+3.5V. After startup, the driver will then provide +Vg and -3.5V gate drive signal.

When Q1 is turned on, short circuit happens. The voltage at pin 2 of J6 is Vds, which is equal to Rds_on x short-circuit current. The I_{DESAT} flowing out of the DESAT pin charges up the blanking capacitor and partially passes through series resistor R2 and the high voltage blocking diode D1. With the increase of short circuit current, both Vds and the DESAT pin voltage rise coordinately. When DESAT voltage rises above the 9.5V threshold voltage, a fault is detected and OUT is pulled low.

Figure 11 and figure 12 show at 3.26us the short circuit current increases to 105A, and DESAT pin voltage rises above threshold voltage 9.5V. /FAULT signal, DESAT and OUT are then all pulled low.

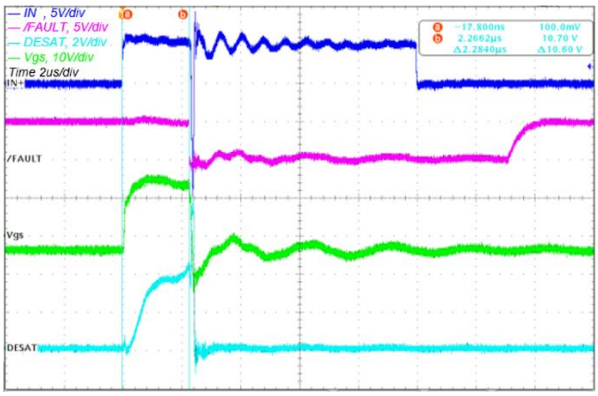

Figure 11. DESAT protection for short circuit

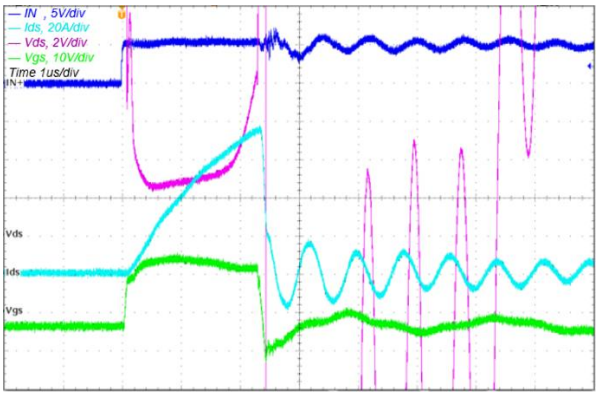

Figure 12. DESAT protection for short circuit

5.3 Negative Voltage Build Up and Under Voltage Protection

IVCR1401 features a unique built-in 3.5V negative bias. At power up, NEG pin pulls low to ensure the power device stays off and at the meantime provides a current path to charge up the negative voltage capacitor quickly. Fig. 13 shows a 1uF negative bias capacitor can be charged up to 3.5V in around 28us. The negative voltage is also monitored in real time. Figure 14 shows a short circuit occurring at the negative voltage

capacitor can trigger circuit protection and issue a fault by pulling /FAULT pin low. The negative voltage recovers in around 28us once the fault condition is removed.

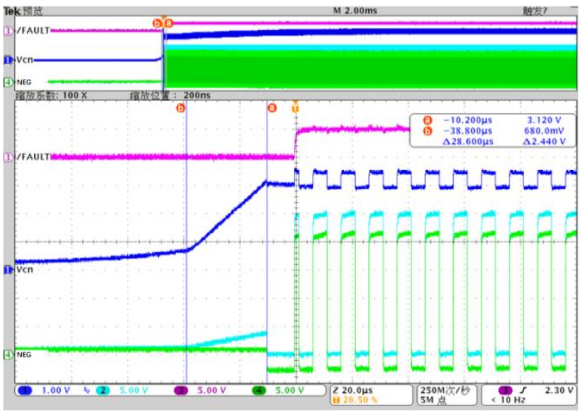

Figure 13. Negative voltage buildup

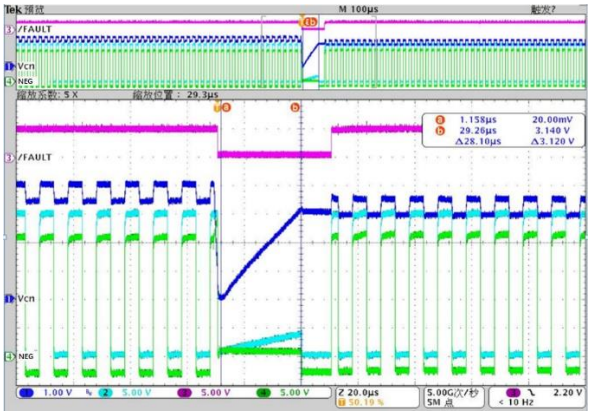

Figure 14. Negative voltage UVLO

DISCLAIMER

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Users should read the Documentation and, specifically, the various hazard descriptions and warnings contained in the Documentation, prior to handling the board. The Documentation contains important safety information about voltages and temperatures. Users assume all responsibility and liability for the proper and safe handling of the board. Users are responsible for complying with all safety laws, rules, and regulations related to the use of the board. Users are responsible for establishing protections and safeguards to ensure that a user's use of the board will not result in any property damage, injury, or death, even if the board should fail to perform as described, intended, or expected, and ensuring the safety of any activities to be conducted by the user or the user's employees, affiliates, contractors, representatives, agents, or designees in the use of the board. User questions regarding the safe usage of the board should be directed to IVCT at www.inventchip.com.cn.