IVCR2401 EVM User's Guide

This user's guide describes the IVCR2401 evaluation module (EVM), providing necessary information for the driver test setup and performance evaluation. This document contains the EVM schematic, bill of materials (BOM), assembly drawing, and board layouts.

Contents

List of Figures

List of Tables

1 Introduction

The IVCR2401 EVM is a high-speed dual-channel MOSFET and IGBT driver evaluation module. It provides a test platform for a quick and easy startup and performance evaluation of the IVCR2401 driver. The EVM is powered by a 20V external supply and features a comprehensive set of test points and jumpers. It is easy to use enable function to enable or disable each output independently or enable parallel function to increase current-drive capability by connecting corresponding jumpers.

1.1 IVCR2401 Applications

- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC
- PV boosters and inverters
- UPS

2 Schematic, Bill of Materials and Layout

This section provides a detail description of the IVCR2401 EVM schematic, bill of materials (BOM) and layout.

2.1 IVCR2401 EVM Schematic

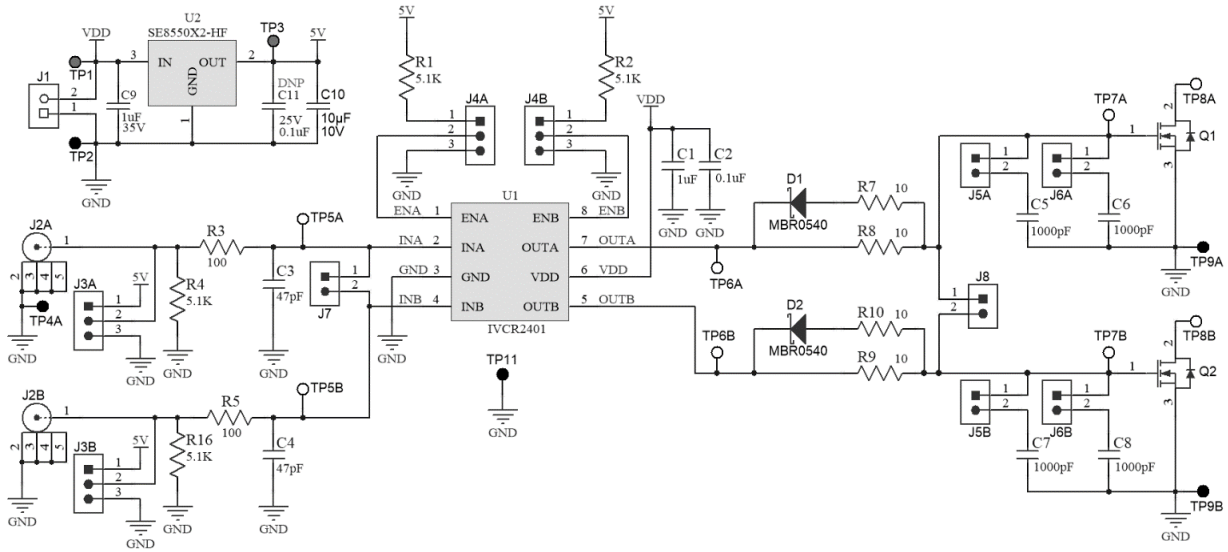

Figure 1. IVCR2401 EVM Schematic

2.2 IVCR2401 EVM Bill of Materials

Table 1. BOM

	Designator	Part Number	Description	Footprint	Quantity	DNP
1	C1, C9	GMK107BJ105KA-T	CAP CER 1UF 35V X5R 0603	0603	1	
2	C2	0603B104K500NT	CAP CER 0.1UF 50V X7R 10% 0603	0603	1	
3	C11	0603B104K500NT	CAP CER 0.1UF 50V X7R 10% 0603	0603	1	DNP
4	C3, C4	0603CG470J500NT	CAP CER 47PF 50V 0603 SMD	0603	2	
5	C5, C6, C7, C8	CL10B102KB8NNNC	CAP CER 1000PF 50V X74 10% 0603	0603	4	
6	C10	CL21A106KPFNNNE	CAP, CERM, 10 µF, 10 V, +/- 10%, X5R, 0805	0805_HV	1	
7	D1, D2	MBR0540	DIODE SCHOTTKY 40V 500MA SOD123	SOD-123	2	
8	J1	KF350-2P	TERM BLK 2POS SIDE ENT 3.5MM PCB	KF350-2P	1	
9	J2A, J2B	112404	Connector, TH, BNC	Amphenol_112404	2	
10	J3A, J3B, J4A, J4B	TSW-103-07-G-S	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	4	
11	J5A, J5B, J6A, J6B, J7, J8	5-146261-1	Header, 100mil, 2x1, Gold, TH	HDR1X2	6	
14	Q1, Q2	C2M0025120D	MOSFET, N-CH, 1200 V, 90 A, TO-247	TO-247	2	DNP
15	R1, R2, R4, R16	0805W8J0512T5E	RES 5.1K OHM 1/4W 5% 0805	0805	4	
16	R3, R5	RTT03101JTP	RES 100 OHM 1/10W 5% 0603	0603	2	
17	R7, R8, R9, R10	0805W8F100JT5E	RES 10 OHM 1/8W 1% 0805 SMD	0805	4	
18	TP1, TP3	5000	Test Point, Miniature, Red, TH	KEYSTONE5000	2	DNP
19	TP4A, TP9A(S1), TP9B(S2), TP11	5001	Test Point, Miniature, Black, TH	KEYSTONE5001	4	
20	TP2	5001	Test Point, Miniature, Black, TH	KEYSTONE5001	1	DNP
21	TP5A, TP5B, TP6A, TP6B, TP7A(G1), TP7B(G2)	5002	Test Point, Miniature, White, TH	KEYSTONE5002	6	
22	TP8A(D1), TP8B(D2)	5002	Test Point, Miniature, White, TH	KEYSTONE5002	2	DNP
23	U1	IVCR2401	IC GATE DVR IVCR2401 8SOIC	SOIC8	1	
24	U2	SE8550X2-HF	IC LDO INPUT MAX 36V OUTPUT 5V 250MA SOT23-3	SOT23-3	1	

2.3 Layout and Component Placement

Figure 2 and figure 3 show top and bottom assemblies of the printed circuit board (PCB) on the EVM. Figure 4 and figure 5 show the top and bottom layouts.

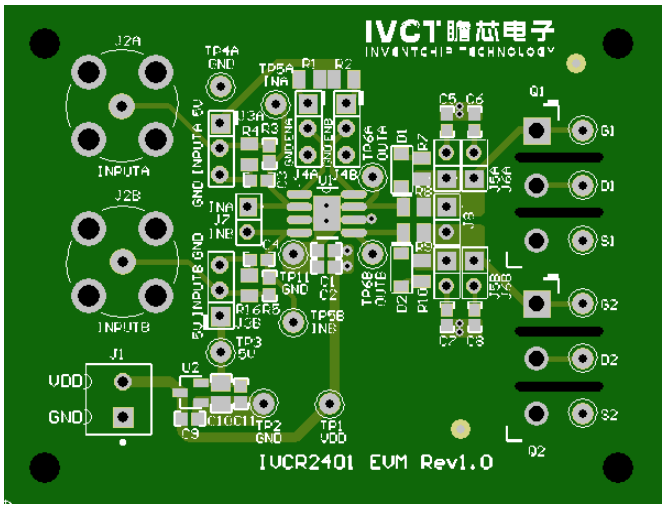

Figure 2. Component Placement — Top Assembly

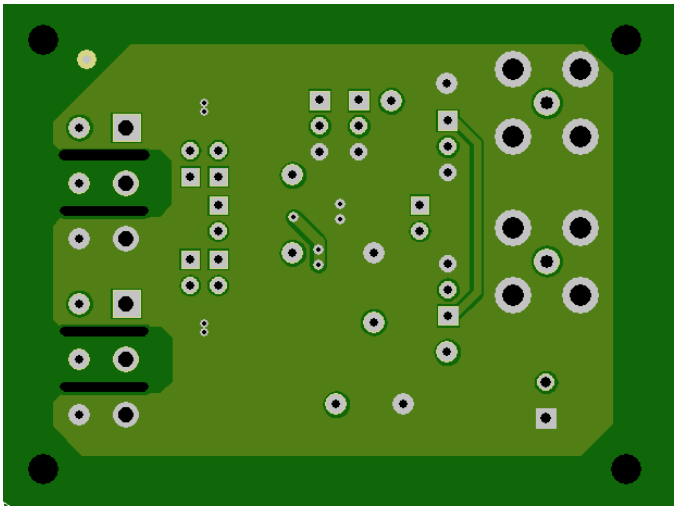

Figure 3. Component Placement — Bottom Assembly

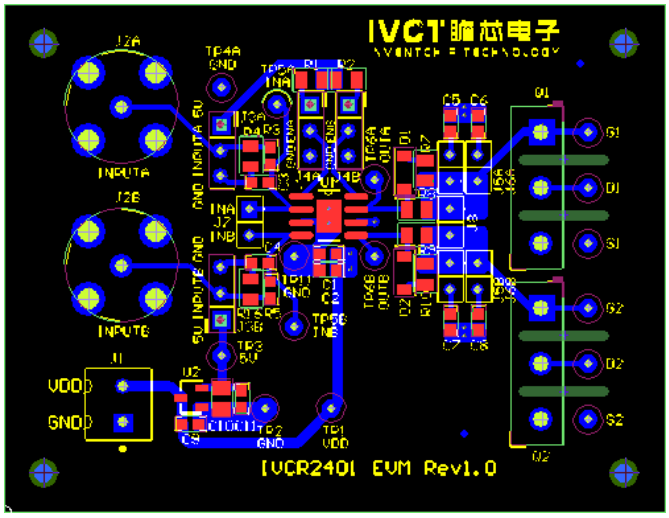

Figure 4. Layout — Top

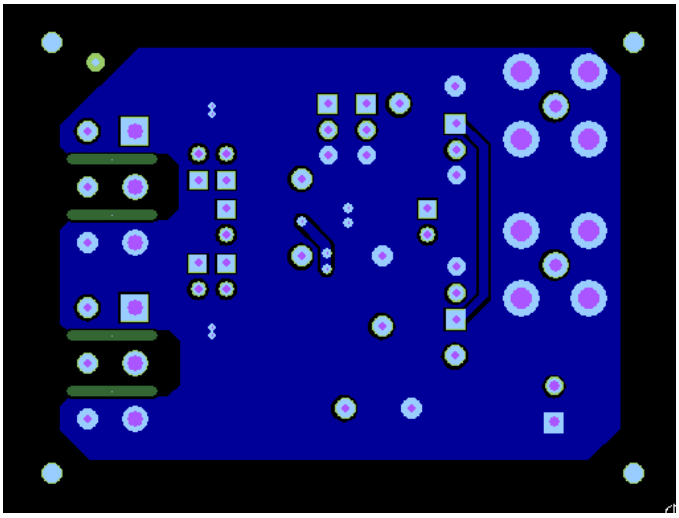

Figure 5. Layout — Bottom

3 EVM Connectors, Test Points and Jumpers

This section describes the connectors, test points and jumpers on the EVM as well as how to configure the test board.

3.1 EVM connectors

Table 2 lists the following connectors and headers on the IVCR2401 EVM.

Table 2. List of Onboard Connectors and Headers

Connectors/Headers	Silkscreen Label	Function	Description
J1	VDD, GND	Power supply	Power supply connector for the device.
J2A	INPUTA	A channel arbitrary input signal	A channel arbitrary input signal from BNC connector for the device.
J2B	INPUTB	B channel arbitrary input signal	B channel arbitrary input signal from BNC connector for the device.
J3A	5V, INPUTA, GND	A channel high-level or low-level input signal	If INPUTA (Pin 2) connected to 5V (Pin 1), INA is in a high-level input; If INPUTA (Pin 2) connected to GND (Pin 3), INA is in a low-level input.
J3B	5V, INPUTB, GND	B channel high-level or low-level input signal	If INPUTB (Pin 2) connected to 5V (Pin 1), INB is in a high-level input; If INPUTB (Pin 2) connected to GND (Pin 3), INB is in a low-level input.
J4A	ENA, GND	Enable or disable A channel	Connect ENA (Pin 2) to GND (Pin 3) to disable A channel. Otherwise, connect ENA (Pin 2) to Pin 1 or leave it floating.
J4B	ENB, GND	Enable or disable B channel	Connect ENB (Pin 2) to GND (Pin 3) to disable B channel. Otherwise, connect ENB (Pin 2) to Pin 1 or leave it floating.
J7	INA, INB	INA and INB have a same input signal or not	If J7 connected, INA and INB will have a same input signal.
J8	/	Two channels in parallel	Two channels will be paralleled if J8 is connected.

3.2 EVM Test Points

Table 3 lists the test points and functional descriptions. All pins of the device are brought out to test points on the EVM.

Table 3. Test Points

Test Point	Silkscreen Label	Function	Description
TP1	VDD	Power supply	Power supply for the device
TP2, TP4A, TP11,	GND	Ground	Connected with ground
TP3	5V	5V power supply	5V High level for INA, INB, ENA or ENB
TP5A	INA	INA input signal	Connected with INA pin
TP5B	INB	INB input signal	Connected with INB pin
TP6A	OUTA	OUTA output signal	Connected with OUTA pin
TP6B	OUTB	OUTB output signal	Connected with OUTB pin
TP7A	G1	Q1 gate	Connected with Q1 gate
TP7B	G2	Q2 gate	Connected with Q2 gate
TP8A	D1	Q1 drain	Connected with Q1 drain
TP8B	D2	Q2 drain	Connected with Q2 drain
TP9A	S1	Q1 source	Connected with Q1 source
TP9B	S2	Q2 source	Connected with Q2 source

3.3 EVM Jumpers

Table 4 lists the Jumpers on the IVCR2401 EVM. As ordered, the EVM has four jumpers pre-installed.

Table 4. List of Onboard Jumpers

Jumper	Default Connection	Description
J5A, J6A	CloadA is 1000pF+1000pF	Connect C5 and C6 between Q1 gate and source
J5B, J6B	CloadB is 1000pF+1000pF	Connect C7 and C8 between Q2 gate and source

4 EVM Setup and Operation

This section describes the functionality and operation of the IVCR2401 EVM.

4.1 Test Equipment

The test equipment includes:

DC Power Supply —— DC power supply capable of providing 20V.

Function Generator —— Function Generator with at least two channels capable of providing 0V/5V 50kHz square wave.

Oscilloscope —— Oscilloscope with four channels of analog type capable of 100MHz bandwidth or better with high-impedance scope probes capable of handling minimum 50V.

Multimeter —— Digital multimeter capable of monitoring input DC voltages, or other nodes around the EVM.

4.2 Recommended Test Setup and Operating Conditions

Figure 6 shows the EVM test setup. Table 5 lists the recommended operating conditions.

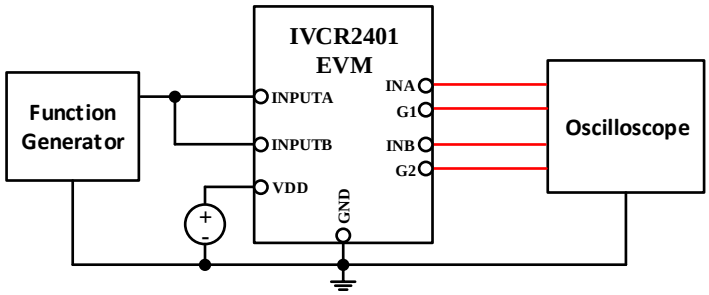

Figure 6. Recommended Test Setup

Table 5. Recommended Operating Conditions

Parameter		Min	Max	Unit
VDD	Supply voltage	8	20	V
INA	Input voltage	0	15	V
INB				
ENA	Enable voltage	0	15	V
ENB				
T_A	Operating ambient temperature	25 (typical)	/	°C

4.3 EVM Setup and Power-Up Procedure

To power up the EVM, follow the following steps:

Step 1. Power up the board by applying 20V to VDD and set the current limit between 0.1A and 0.2A.

Step 2. Connect the function generator outputs to INPUTA and INPUTB and adjust the function generator to produce PWM signals between 0V and 5V at a desired frequency and duty cycle.

Step 3. Connect the scope's probes to test point G1 and G2 and measure the gate signal waveforms at the load points.

Note: due to the driver's high-speed driving capability, to capture a clean waveform, it is recommended to keep the probe's ground as short as possible, and the scope's bandwidth should be set at as high as needed.

5 Performance Data, Test Verification Waveforms and Typical Characteristic Curves

5.1 Propagation Delay, Rise and Fall Times

Figure 7 shows measurement of the propagation delay, rise and fall times.

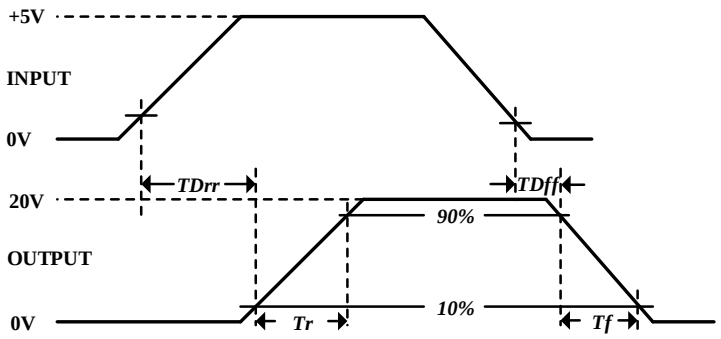

Figure 7. Switching Waveforms

The load capacitance testing condition is 2nF, VDD=20V. The driver input signals INPUTA and INPUTB are set to 5V with f=50kHz. Table 7 lists the EVM test results.

Table 6. EVM Test Results

Delay Time, IN Rising (IN to OUT)	Delay Time, IN Falling (IN to OUT)	Rise Time	Fall Time
50 ns	48 ns	45 ns (Rg_on=10Ω, Rg_off=5Ω)	24 ns (Rg_on=10Ω, Rg_off=5Ω)

Note: Due to gate driver resistor Rg, the rise time and fall time are longer than Datasheet values.

Figure 8 and Figure 9 show the propagation delay, rise time and fall time measurements on the EVM.

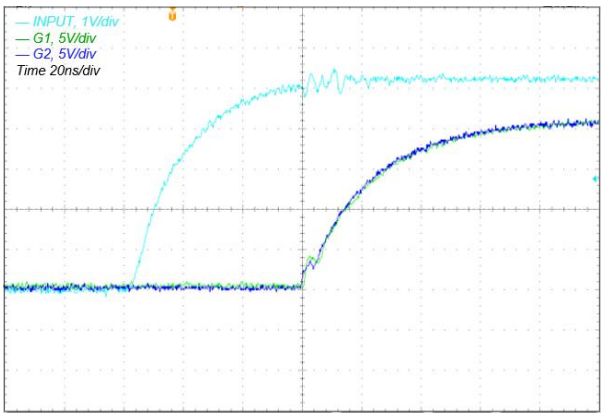

Figure 8. IVCR2401 Input Rising

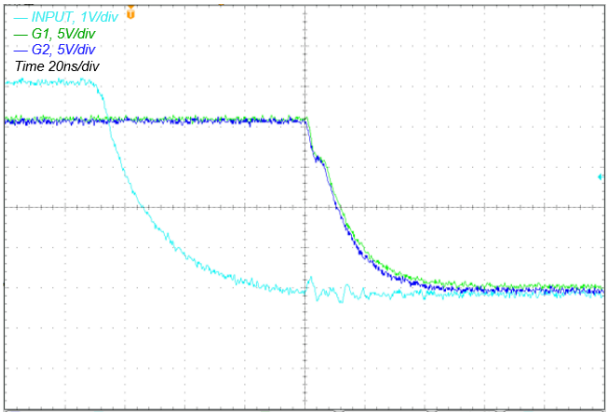

Figure 9. IVCR2401 Input Falling

5.2 Synchronous Function

When only one Enable pin is tied to high, both channel's output stages are driven by the same logic signal. This unique feature reduces channels' mismatching significantly and makes the driver very suitable for paralleled switches' driving. The following three configurations and tests demonstrate this feature.

When ENA and ENB are floating, and the input signal INB delays INA by 5us, the output signal G1 follows INA and G2 follows INB, as shown in Fig. 10. When ENA is connected to a high-level logic and ENB is left floating, both outputs G1 and G2 follow INA as shown in Fig. 11. When ENB is connected to a high-level logic and ENA is left floating, as shown in figure 12, both output signals G1 and G2 are follow INB.

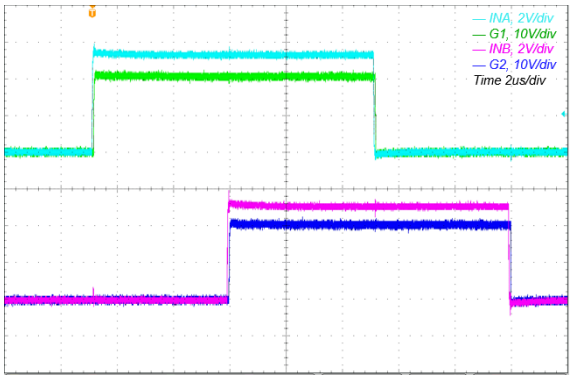

Figure 10. ENA and ENB both floating

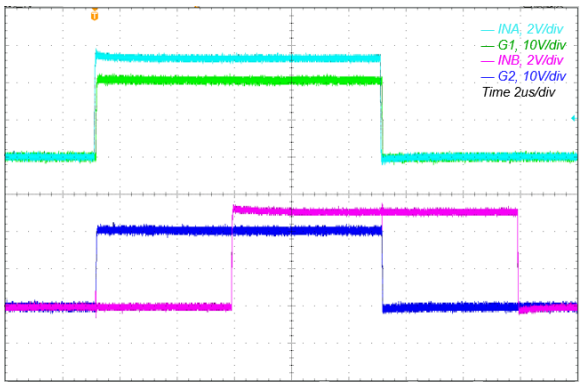

Figure 11. ENA tied to a high logic level and ENB floating

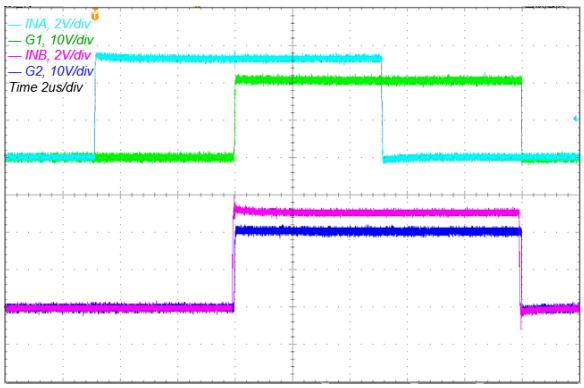

Figure 12. ENB tied to a high logic level and ENA floating

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