pcim ASIA Hybrid Platform

SiC-Based High Density Charger Pile Module Design

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Contents

- EV/HEV charger market
- State of the art of charger pile power module design and wish list
- A proposed new battery charger power architecture
- SiC -based topology selection and driver circuit requirement
- Test data
- Conclusions

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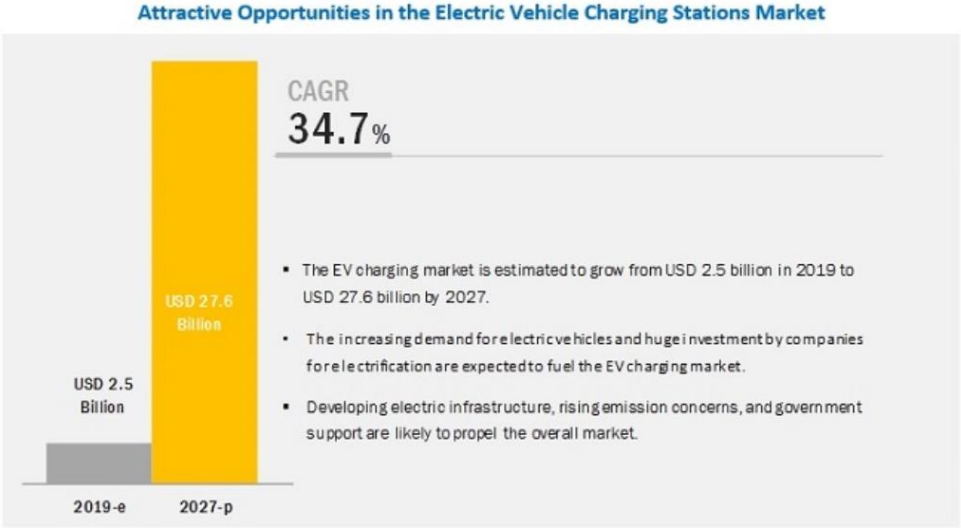
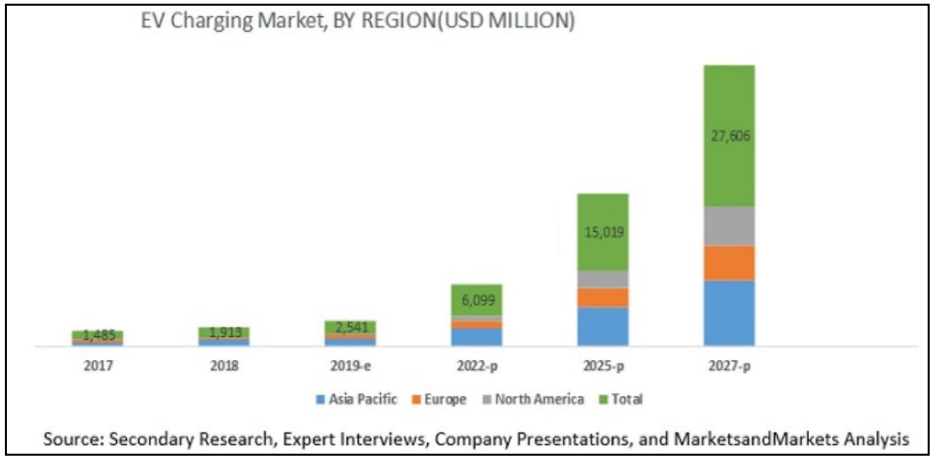
Global EV/HEV Charger Station Market

USD 27.6 Billion by 2027





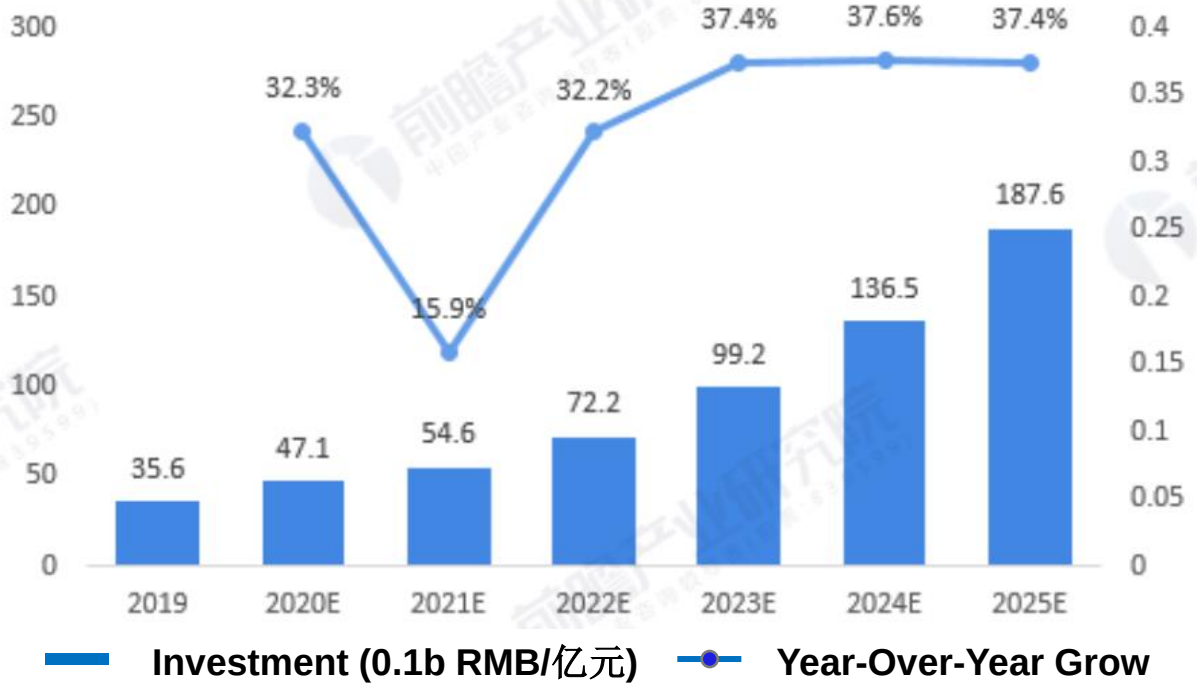
Asia pacific will command near 50% of the market.

Source:

https://www.marketsandmarkets.com/Market-Reports/electric-vehicle-supply-equipment-market-89574213.html

China EV/HEV Charger Pile Market

2019-2025 China Public Charger Pile Investment



Majority of Charger Points:

60kW DC Chargers
7kW AC Chargers

Source: https://www.qianzhan.com/analyst/detail/220/200609-4351a819.html

EV Charger Market Is Moving

- More charger stations are built into convenient but expensive commercial urban areas
- Shorten charging time
- Deteriorated commercial environment (dust, moisture)

- Increase charger point's power
- Increase power density
- Higher charger module reliability

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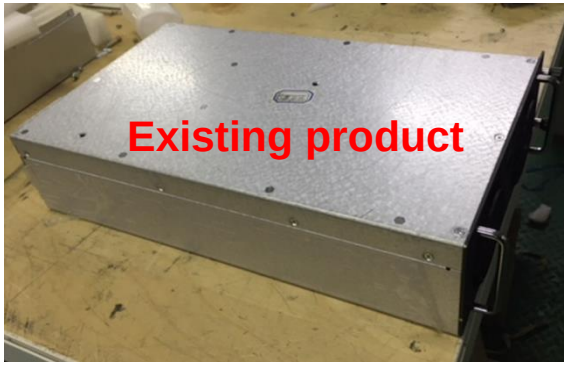
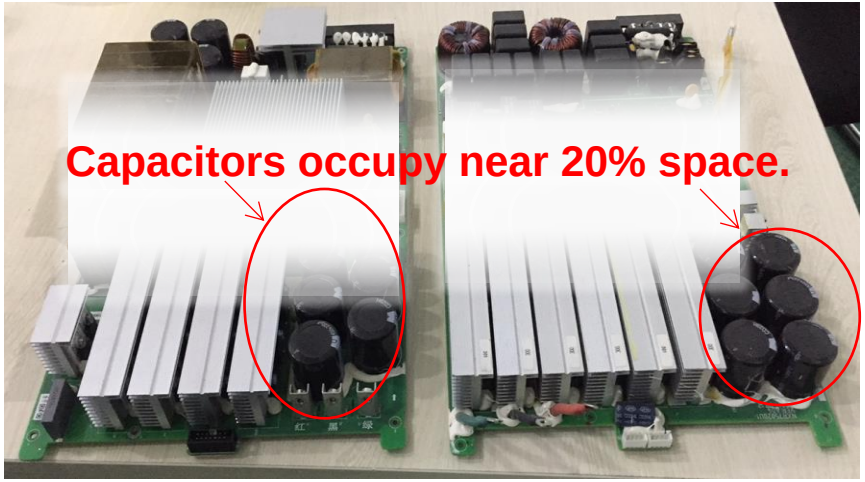
Design Target





State-of-the-Art Design:

20kW in 2U x 5U x 9U (41W/q.In, 2.5kW/q.dm)
2-board structure (PFC board & DC/DC board)

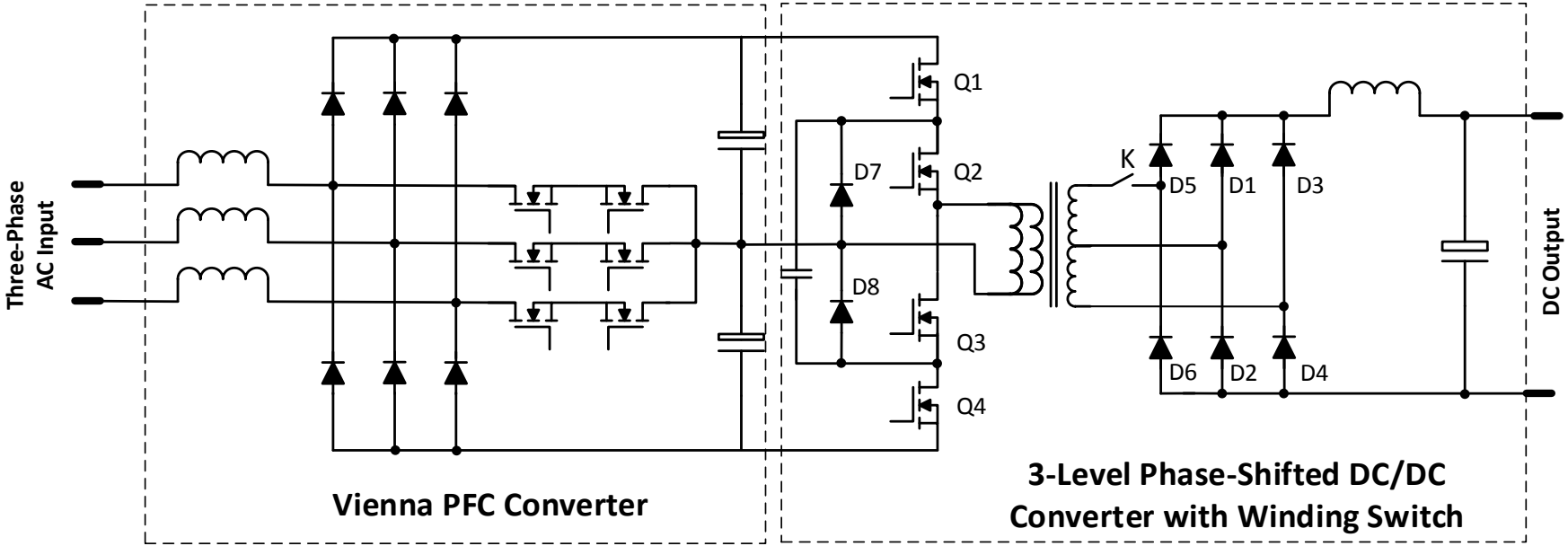
New Design and Targets:

20kW in 1U x 5U x 9U
Reduce or eliminate internal bus capacitance
One board structure
Reduce passive component and assembly cost

New Design Approach:

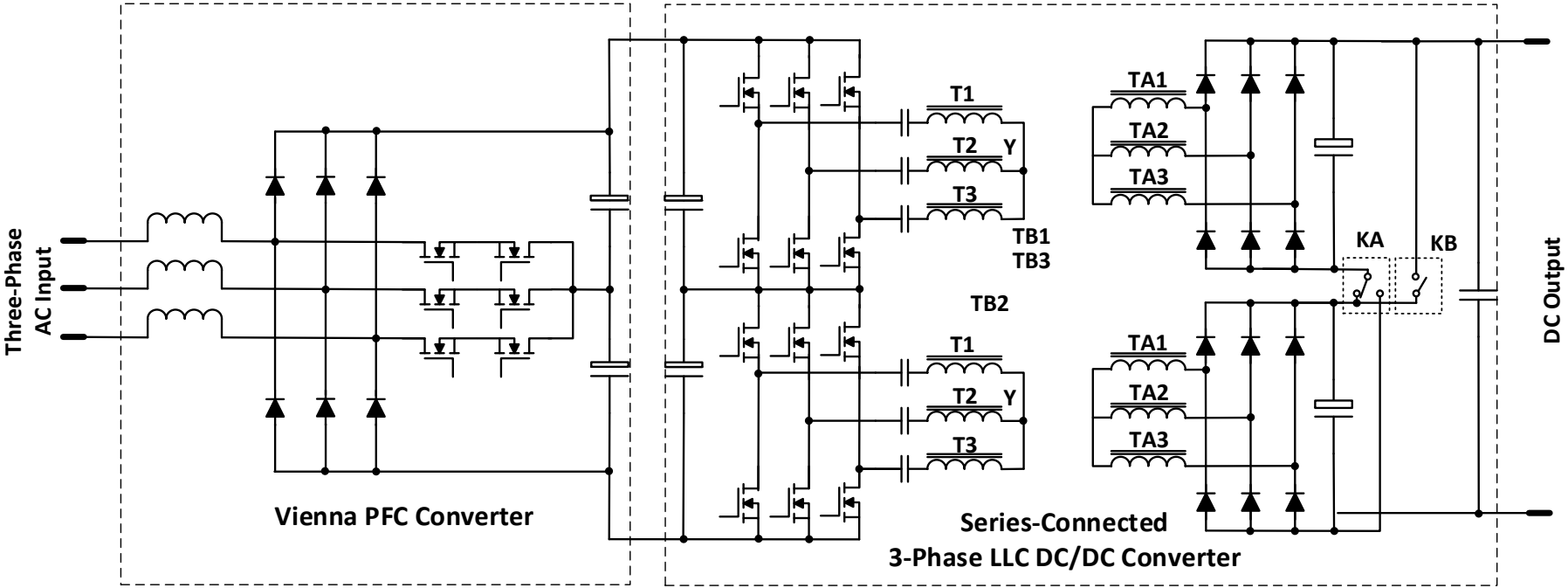
Increase frequency without sacrificing efficiency
Use simply 2-level topologies
Use SiC MOSFETs
Use new power architecture to reduce bulk caps.

Topologies Used in Existing Design



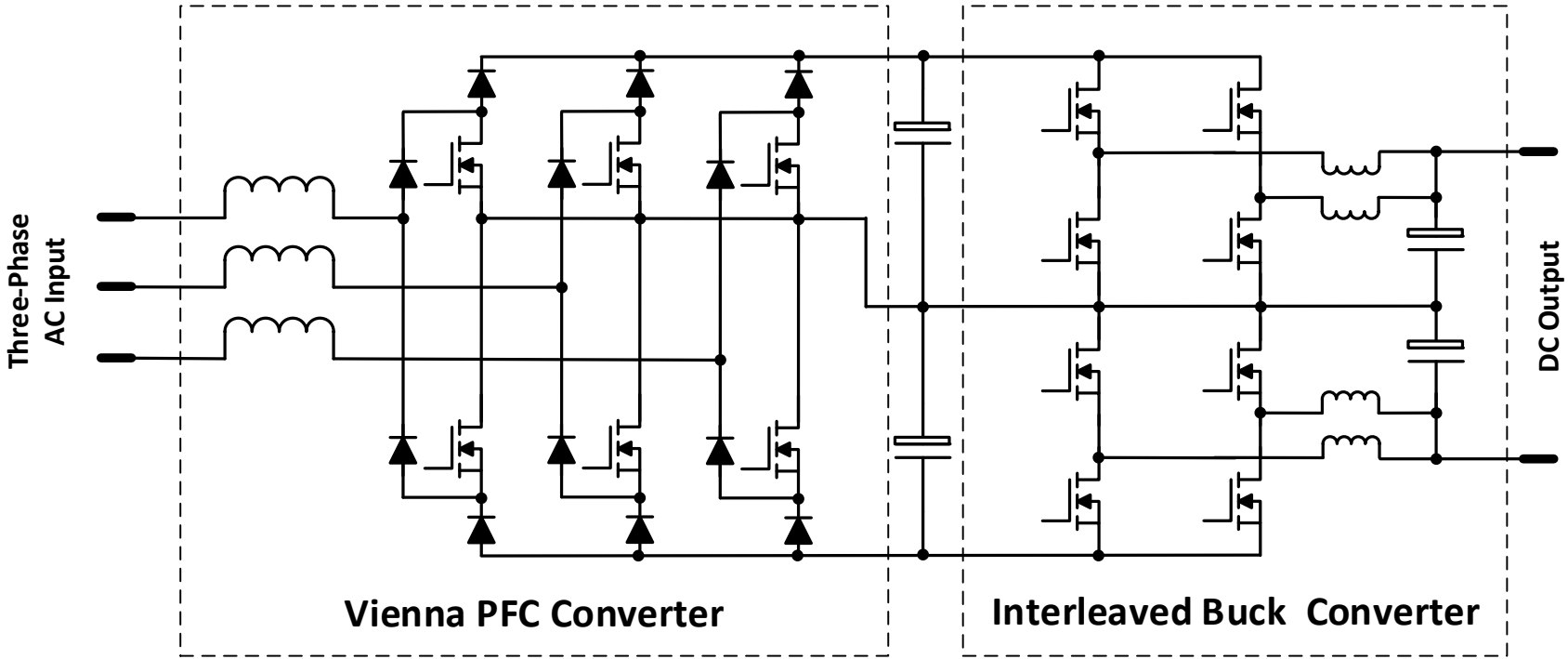
Topology I: Vienna PFC + 3-Level Phase-Shifted DC/DC

Topologies Used in Existing Design



Topology II: Vienna PFC + Series-Connected 3-Phase LLC DC/DC

Topologies Used in Existing Design



Topology III: 3-Level PFC + Series-Connected Buck DC/DC

Design Challenging to Improve Power Density

- Vienna PFC and 3-Level PFC achieve excellent efficiency but bulk capacitors are needed to maintain circuit stability.
- Topology III achieves excellent efficiency, power density and wide Vo range with constant power capability. For safety reason, a front line-frequency isolation transformer would be required.
- Wide output voltage range is required to accommodate variety ranges of EV charging voltages
- Constant power capability for full Vo range

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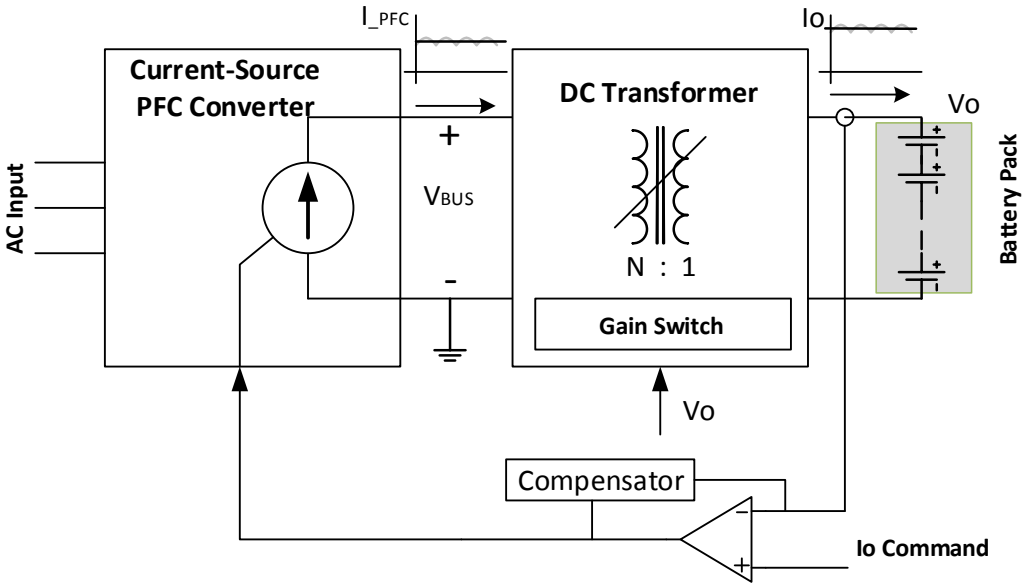
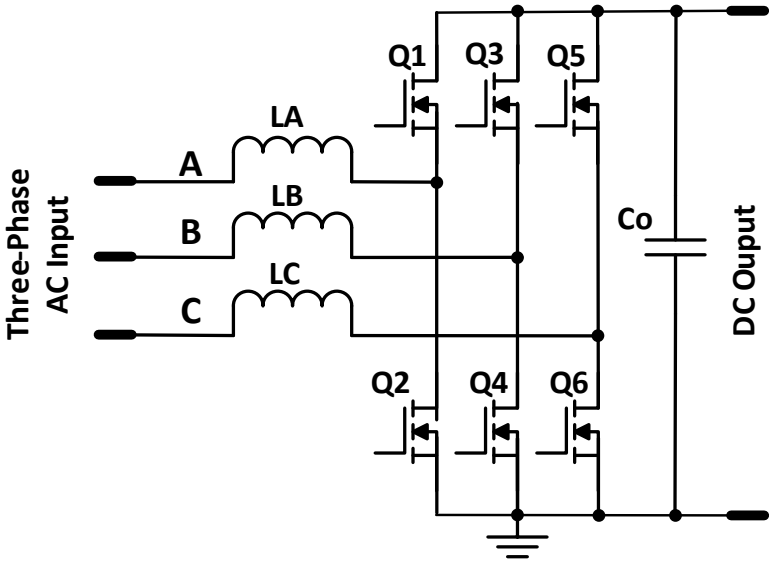
Proposed Power Architecture



- Battery acts as a super capacitor
- DC-X operates at optimal eff point
- PFC operates at current source mode
- PFC current charges battery by DC-X
- PFC output is clamped by reflected battery voltage
- Limited film capacitors needed for PFC output and DC/DC input current ripples

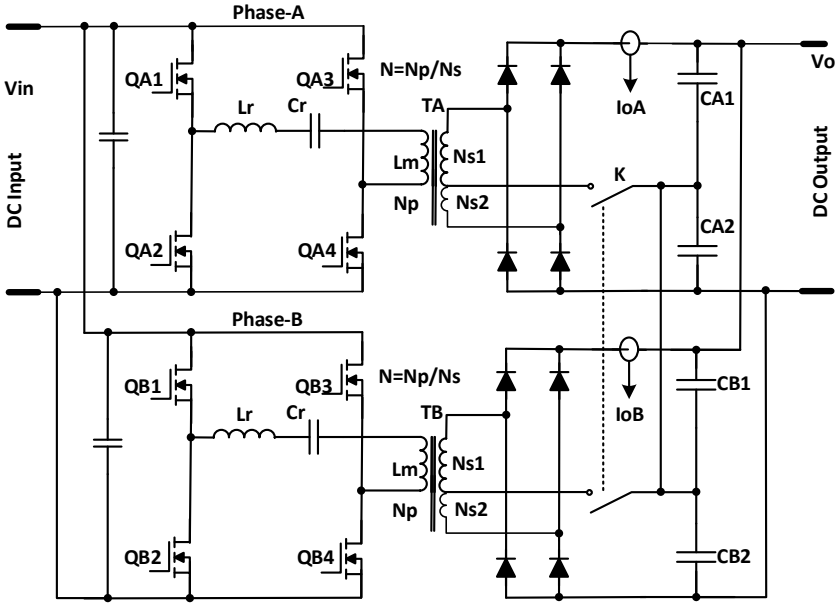
PFC Stage of the Proposed Power Architecture

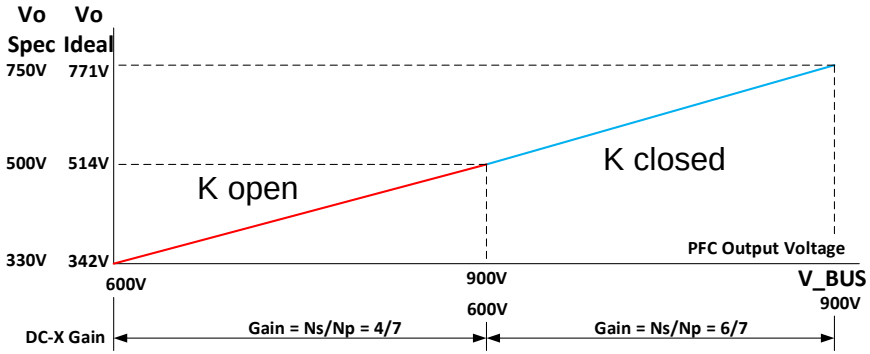


$$Po = 2V_{rms} \cdot I_{rms} \left[Sin^2(\omega t) + Sin^2(\omega t + 2\pi/3) + Sin^2(\omega t - 2\pi/3) \right]$$
$$= 3 \cdot V_{rms} \cdot I_{rms}$$

- For the ideal case, there exists no line harmonic current at PFC output
- Co is a film capacitor for switching current ripple absorption
- No evidence shows line-harmonic current is harmful to batteries if it does exist.

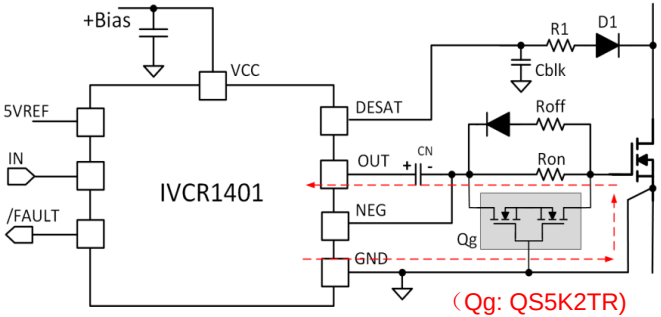
DC-X with Switchable Gains





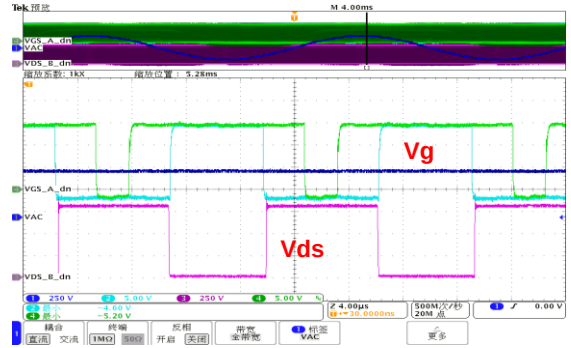
- PFC output voltage able to range from 600V to 900V with 1200V SiC MOSFETs.
- DC-X output ranges from 330V to 500V or from 500V to 750 by switching gains between 4/7 and 6/7.
- DC output becomes voltage doubler when relay K is closed, and the Vo switches from the low voltage range to high voltage range.

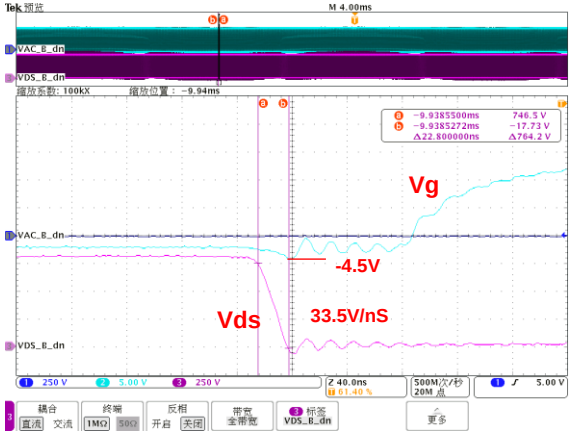
Reliable Gate Drivers Play a Key Role



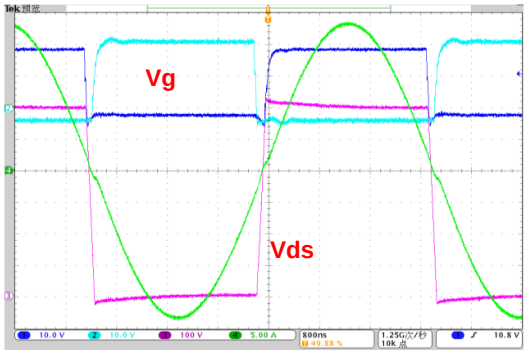
- Integrated negative bias
- Desat OCP
- Optional active Miller Suppression

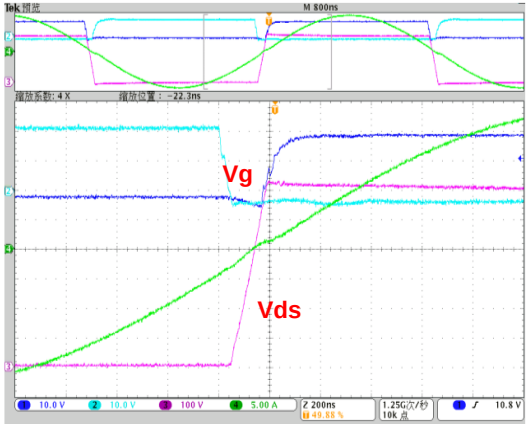
PFC Waveform (TO-247-4L)





LLC Waveform (TO-247-3L)



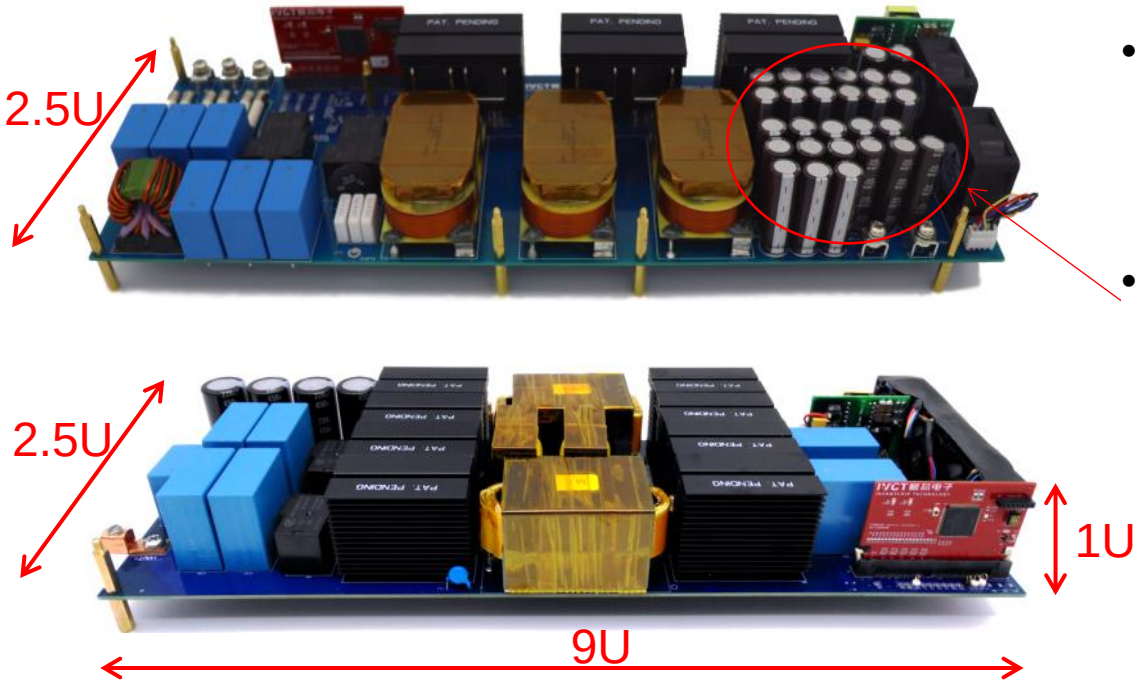


SiC MOSFETs

PFC: 50mOhm 1200V (IV1Q12050T4)

LLC: 50mOhm 1200V (IV1Q12050T3)

20 kW Charger Pile Module Prototype



- One 1U x 5U x 9U board is broken into two boards to facility lab test
- PFC output capacitors are installed so PFC can be debugged independently

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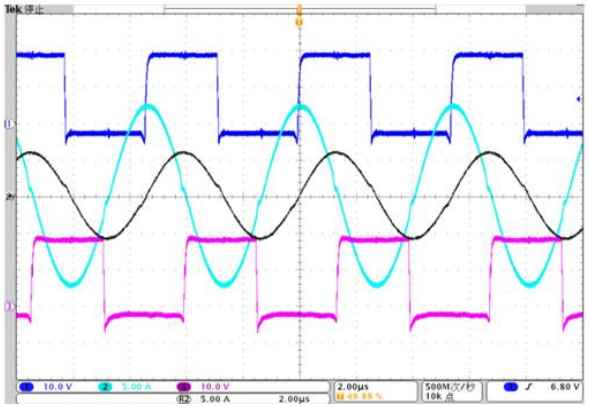
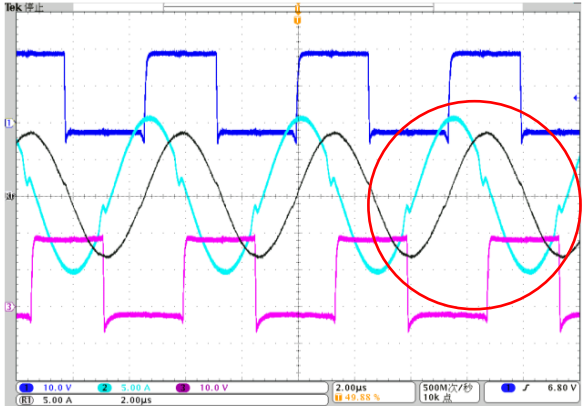
Paralleled LLC Current Balancing Control

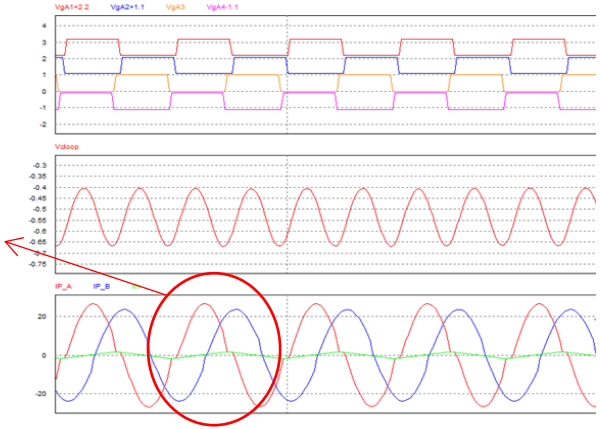
- To avoid beat-frequency current ripple, paralleled LLC converters must operate at the same frequency
- Different resonant frequencies would result in different output current or power
- For full bridge LLC converters, phase-shifting control can be used to balance their output current



Before current balancing control is enabled.



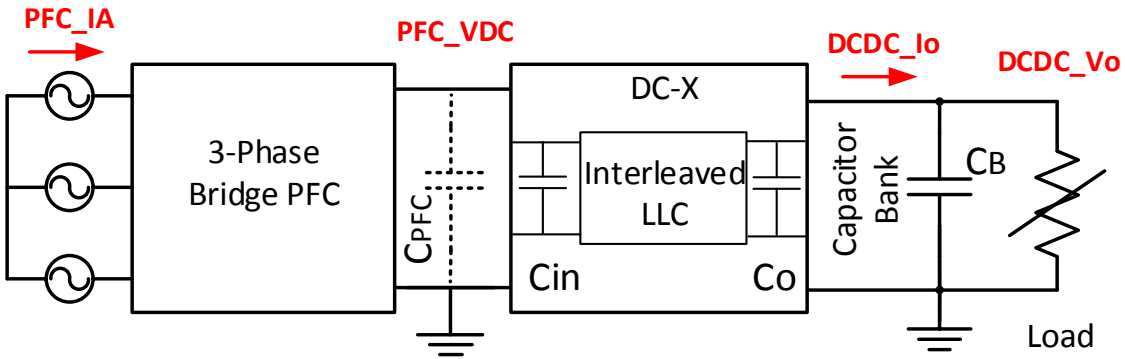
Current balancing control is enabled.

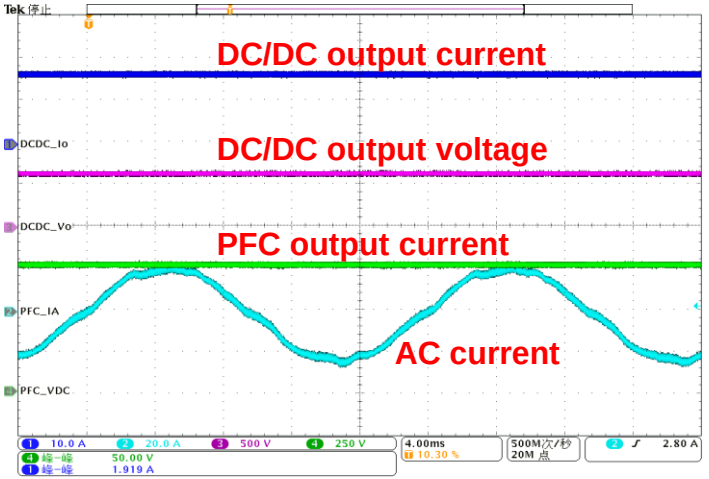


Current balancing control simulation with +/- 10% resonant inductance variation.

Note: Even the resonant currents may not have the same amplitude, their output currents actually reach the same average value.

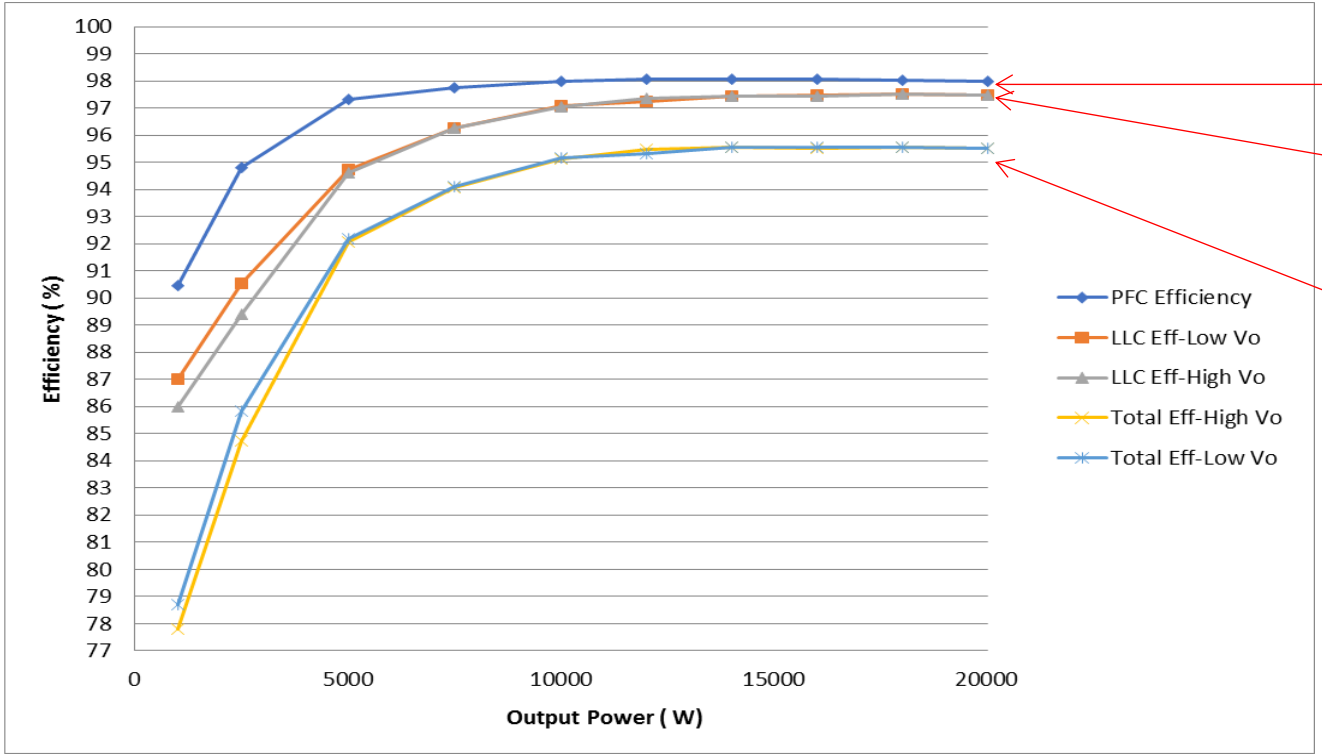
PFC and DC/DC System Test Setup





- A 20x2x330uF/450V capacitor bank is connected at DC output to emulate a battery pack.
- PFC output capacitance was reduced to 68uF (electrolytic capacitors)
- DC-X input capacitors are 2x12uF (film capacitors)

Prototype Efficiency



PFC at 65kHz

LLC at 180kHz

Almost the same eff for high and low Vo outputs – good for constant power operation

400V Vac input， 435V and 655V outputs

Design Data Comparison

	Product A	Product B	Inventchip Prototype
Size	2Ux5Ux9U	2Ux5Ux9U	1Ux5Ux9U
Power	20kW	20kW	20kW
Topologies	Vienna + 3-Level Phase-shifted full bridge	Vienna + Series-Connected 3-phase LLC	3-phase PWM PFC+ 2-Level Interleaved LLC
PFC fs DC/Dc fs	20kHz 70kHz	24kHz fr: 107kHz 75 – 350kHz	65kHz 180kHz
Constant Power	No (constant current)	Yes	Yes
Power Devices	SiC diodes + Si MOSFETs +FRDs	SiC diodes + Si MOSFETs +FRDs	SiC MOSFETs + SiC Diodes
Peak Efficiency	95.5% Peak 95.0% Full load	96% Peak 95.3% Full load	95.5% Peak and full load

Merits of The Proposed Architecture

- Improve power density
- Reduce PFC output capacitance
- 2-3 times switching frequency improvement
- 2-level topologies simplify circuit design
- Good efficiency at high switching frequency

Conclusions

- The proposed power architecture was validated
- The new power architecture is a promising approach to further improve charger pile power density
- Reducing or eliminating PFC output capacitance is the key to improve power density and reliability and lower cost
- SiC MOSFETs enable 2-level topology applications and improve power density

Future work:

- Investigate different PFC control to reduce switching loss and common mode noise
- Fine tune LLC to gain some more efficiency
- Combine PFC and DC/DC in one PFC board and evaluate thermal performance


临港滴水湖
谢谢！
Thank You !